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Mathematical Modeling Techniques for nm-FinFETs DC Characteristics

by

Umer Farooq Ahmed

A thesis submitted in partial fulfillment for the degree of Master of Science

in the

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To my late mama for her unbound affection

CERTIFICATE OF APPROVAL

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MEE173028

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1. **U.F. Ahmed**, S. Rehman, U. Rafique, M.M. Ahmed "AlGaN/GaN FinFET: A Comparative Study," *14th International Conference on Emerging Technologies (ICET)*, Islamabad, Pakistan, pp. 1-6, 2018.

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4. **U.F. Ahmed**, M.M. Ahmed, Q. Memon "A modified analytical model for AlGaN/GaN FinFETs I–V characteristics," *Semiconductor Science and Technology*, pp. 035002, vol. 35(3), 2020.

5. **U.F. Ahmed**, M.M. Ahmed "A Compact Mobility Based $I-V$ Model for FinFETs," *IET Circuits, Devices & Systems*, pp. 1249-1254, vol. 13(8), 2019.

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Abstract

FinFETs are potential candidates for microwave high-tech applications as their 3D structure allows effective gate control upon the channel, which results into low leakage current and dynamic power loss. Furthermore, FinFETs offer higher integration compared to other mainstream FET technologies thus, keeping the avenue open for further shrinking of integrated circuits.

FinFET is a voltage controlled device and the potential distribution inside the channel of a FinFET is usually determined by a 2D Poisson equation which does not truly describe its variation due to the 3D structure of the FinFET. Since, the geometry of the channel plays an important role in determining its output characteristics, a 3D Poisson equation is, therefore, solved to predict $I-V$ characteristics of Si-FinFETs. It is observed that by adding the third dimension to the Poisson equation, the accuracy of the model is improved. Devices of various dimensions are selected to test the validity of the proposed technique and $6-45\%$ improvement is observed in predicting the $I-V$ characteristics of Si-FinFETs with respect to the best reported model in the literature.

In the 2^{nd} part of this research, potential distribution inside the channel of an independent gate FinFET device is evaluated by adding the effect of channel height. It is observed that the channel height of the device plays an important role in surface potential calculation, especially, in the presence of independent top gate voltages. Using surface potential, an $I-V$ model is developed and tested on devices of different dimensions and a good agreement between modeled and simulated results is demonstrated.

In the 3^{rd} part of this research, an analytical model is developed to predict $I-V$ characteristics of heterojunction FinFETs. The model includes the effect of tri-gate geometry on the sheet carrier density (n_s) of the device, and it has been shown that n_s of a FinFET depletes at a faster rate relative to conventional high electron mobility transistor (HEMT). By using the developed expression of n_s, output and transfer characteristics of AlGaN/GaN FinFETs of varying physical dimensions have been modeled with a high degree of accuracy.

Finally, in the 4^{th} part, a mobility model for FinFETs device output characteristics has been developed. The model incorporates the effect of applied potentials on the carriers' mobility, which is then used to assess the output and transfer characteristics of FinFETs. Particle swarm optimization has been employed to attain optimum values of the model parameters. The developed model has been applied on devices having gate lengths 0.05-1 μm and a good accuracy has been observed.

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Abbreviations

AC	Alternating current
AlN	Aluminum nitride
AlGaN	Aluminum gallium nitride
CAD	Computer aided design
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DELTA	Depleted lean-channel transistor
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
Ge	Germanium
HEMT	High electron mobility transistor
HfO_2	Hafnium dioxide
IC	Integrated circuit
InN	Indium nitride
$I - V$	Current-voltage
MBE	Molecular beam epitaxy
MESFET	Metal semiconductor field effect transistor
MOCVD	Metal organic vapor phase epitaxy
MOSFET	Metal oxide semiconductor field effect transistor
MG-FinFET	Multi-gate FinFET
PSO	Particle swarm optimization
RF	Radio frequency

RMSE	Root mean square error
SCE	Short channel effect
Si	Silicon
SiC	Silicon carbide
SOI	Silicon on insulator
SONOS	Silicon oxide nitride oxide silicon
SPICE	Software process improvement and capability determination
SRAM	Static random access memory
TCAD	Technology computer aided design
VLSI	Very large scale integration
2DEG	2 dimensional electron gas
5G	5^{th} generation
1D	1 dimensional
2D	2 dimensional
3D	3 dimensional

Symbols

c_i	Constants of integration
C_{gs}	Gate to source capacitor
C_{gd}	Gate to drain capacitor
C_{ox}	Oxide capacitor
$C_{ox1},\ C_{ox2}$	Oxide capacitor of independent gates
C_{si}	Channel capacitor
d	Top gate to 2DEG distance
E	Electric Field
E_F	Fermi energy
E_c	Conduction band energy
E_v	Valence band energy
E_g	$E_c - E_v$
E_y	y-directed electric field
E_{sat}	Saturation electric field
f_c	Cut-off frequency
f_{max}	Maximum frequency
g_d	Output Conductance
g_m	Transconductance
H_{fin}	Height of fin
h	Plank's constant
I_{on}	On state current
I_{off}	Off state current
I_{ds}	Drain to source current

$I_{ds(lin)}$	Linear region drain to source current
$I_{ds(sat)}$	Saturation region drain to source current
k	Wave vector
k_B	Boltzmann's constant
L_g	Gate length
l	Number of iterations
l_{max}	Maximum iterations
N	Doping density
N_a	Doping concentration
N_b	Body doping
n_i	Intrinsic carrier concentration
n_s	2DEG carrier concentration
P_{ij}	Particle position matrix
P_B	Local best matrix
P_G	Global best matrix
Q_{inv}	Inversion charge
Q_{total}	Total charge
Q_{bulk}	Bulk charge
q	Unit electron charge
T	Temperature
T_{fin}	Thickness of fin
T_{ox}	Thickness of oxide
$T_{ox1},\ T_{ox2}$	Oxide thickness of independent gates
V_j	Particle velocity matrix
V_{ch}	Channel potential
V_{fb}	Flat band voltage
$V_{fb1},\ V_{fb2}$	Flat band voltages due to two independent gates
V_s	Source voltage
V_d	Drain voltage
V_g	Gate voltage
V_{g1}	Gate voltage on gate 1

V_{g2}	Gate voltage on gate 2
V_{ds}	$V_d - V_s$
V_{gs}	$V_g - V_s$
V_{gs1}	$V_{g1} - V_s$
V_{gs2}	$V_{g2} - V_s$
$V_{ds(sat)}$	Saturation V_{ds}
V_{th}	Threshold voltage
v	Frequency of radiation
v_d	Carrier velocity
v_{sat}	Carrier saturation velocity
W	Width of fin
W_{eff}	Effective fin width
x, y, z	Rectangular coordinates
x_{dep}	Depletion width
$\alpha, \beta, \gamma, \eta, \lambda, \theta$	Model parameters
$\gamma_1, \gamma_2, \gamma_3$	Model constants
ϵ	Permittivity of free space
ϵ_{si}	Permittivity of silicon
ϵ_s	2DEG permittivity
ϵ_{ox}	Permittivity of oxide
$\epsilon_{ox1},\ \epsilon_{ox2}$	Oxide permittivity of gate 1 and 2
ΔE_c	Bandgap discontinuity
ΔL_g	Channel length modulation
ψ	Surface potential
ψ_d	Surface potential at drain terminal
ψ_s	Surface potential at source terminal
ψ_{d1}, ψ_{d2}	Surface potential due to independent gates at drain side
ψ_{s1}, ψ_{s2}	Surface potential due to independent gates at source side
ψ_{ds}	Surface potential due to V_{ds}
$\psi_{ds(sat)}$	Surface potential due to $V_{ds(sat)}$
ψ_{gs}	Surface potential due to V_{gs}

ψ_0	Mid Channel potential
ϕ_B	Schottky barrier height
ϕ_s	Potential at source terminal
ϕ_d	Potential at drain terminal
σ	Polarization controlled charge density
μ_0	Low field mobility
μ	Mobility
μ_G	Gate dependent mobility
ξ_x, ξ_z	$x-$ and $z-$directed fields
ξ_{x1}, ξ_{x2}	$x-$directed field of independent gates
τ	Transient time

Chapter 1

Introduction

In modern electronics, metal semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs) carry the load of technology. To ensure the daily growing need for improvement, smaller semiconductor devices are being made and utilized extensively. Multiple gate field effect transistors are becoming highly competitive in the modern research field, as they provide a compact solution for high level integrated circuits [1]. Although, multi finger FETs, as evident from their nomenclature, have multiple gates, but they are controlled by a single electrode. Multi finger FETs offer low gate resistance without compromising on channel current technology therefore, they are preferred in low noise applications [2].

MOSFETs were the main protagonist of semiconductor industry for over four decades. Later, MESFETs were introduced and then, there was a shift towards HEMTs. However, in all the mentioned devices, scalability remained a main concern due to drastic increase in sub-threshold current in nanometer regime [3, 4]. In deep sub-micron regime, the drain potential of the device interferes with the electrostatics of the channel and the gate of the device begins to lose control. At the off state, the gate of the device is unable to completely shut the channel down, and as a result, increased leakage current between the drain and the source terminal of the device is observed. In oxide based FET devices, using thinner oxide layer reduces the problem of leakage current however, gate capacitance of the device is

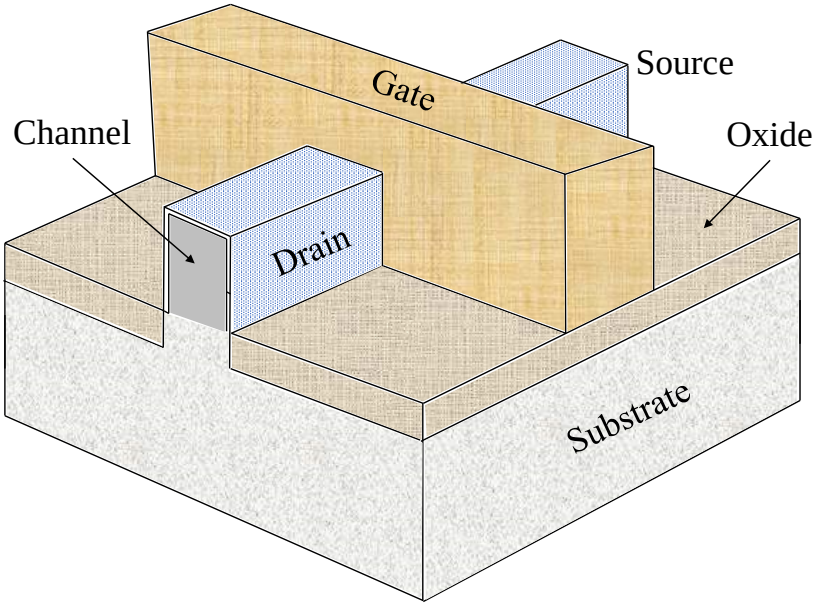

FIGURE 1.1: A multiple gate field effect transistor.

increased and on the other hand, gate induced drain leakage, and deterioration in gate current limits the thinning of gate oxide material [5]. Multi-gate FETs provide the solution for gate leakage current due to their ability to control the channel more efficiently than conventional FETs [2].

Among all the multi-gate FETs, FinFETs are the most relevant and viable option due to their relatively simple device structure as shown in Fig. 1.1, which is also easy to fabricate [6]. FinFET is a non planer 3D transistor having more than one gate [7]. FinFET has a thin fin shaped channel on top of the substrate enveloped by a 3D gate. The contact of the gate is both on the right and left side of the fin. This provides a better electrical control inside the channel and reduces the leakage current. Moreover, the device shrinks extending the validity of Moore's law. FinFETs provide: a) high integration, b) low leakage current and c) reduced short channel effects.

1.1 FinFET Structure

In 1990, Hisamoto et al. [8] presented a fin like transistor. They named it Depleted Lean-channel Transistor (DELTA). Over the years, many improvements have been

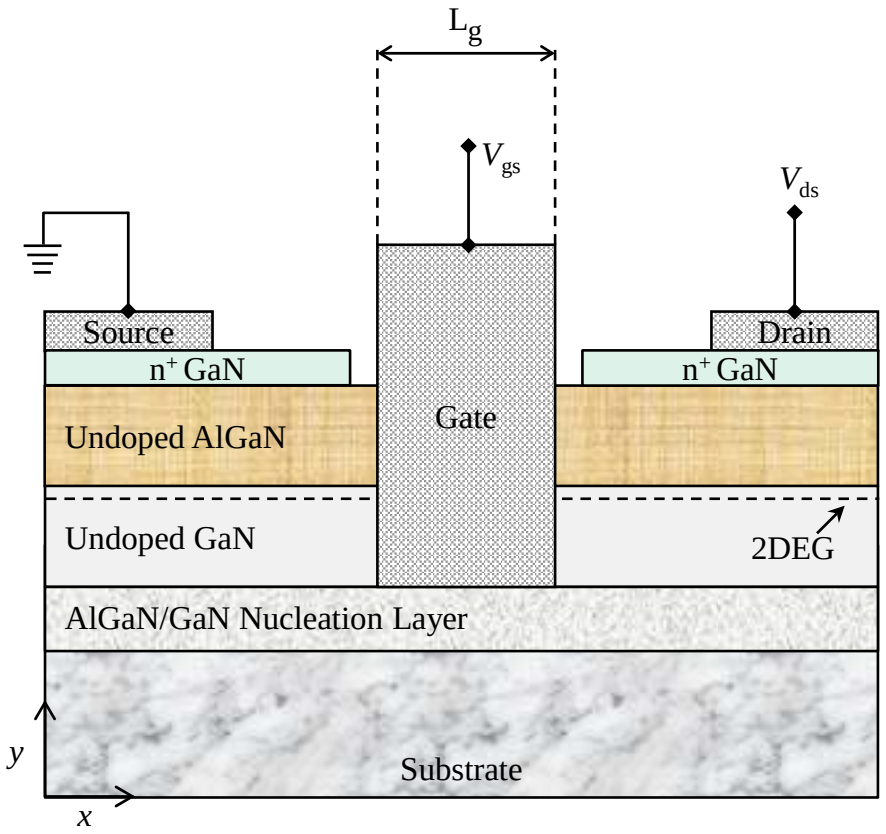

FIGURE 1.2: Typical AlGaN/GaN FinFET structure (Front View).

made to the design of the transistor. The name FinFET was given to the device in 2001, by Huang et al. [9]. There are numerous structures of FinFETs because the devices can be fabricated involving various techniques and materials. A basic structure of an heterojunction FinFET, fabricated using AlGaN/GaN is given in Figs. 1.2 and 1.3. Figure 1.2 gives the front view of the transistor, while Fig. 1.3 provides the right view. The basic structure of the AlGaN/GaN FinFET resembles the structure of a HEMT. The only difference is that the gate envelopes the channel, also called fin, from three sides. The gate provides extra control to the device handling. This is the reason FinFETs are also called tri-gate FETs.

As shown in Figs. 1.2 and 1.3, the height of the channel, H_{fin} determines the width, W of the device. This leads to quantized W of FinFETs. The W of the device must be a multiple of H_{fin} and can be increased by adding parallel fins to the same device. Thus, random variation in W is not possible. Using small H_{fin} is although possible, but not preferred as more wafer is consumed and on the

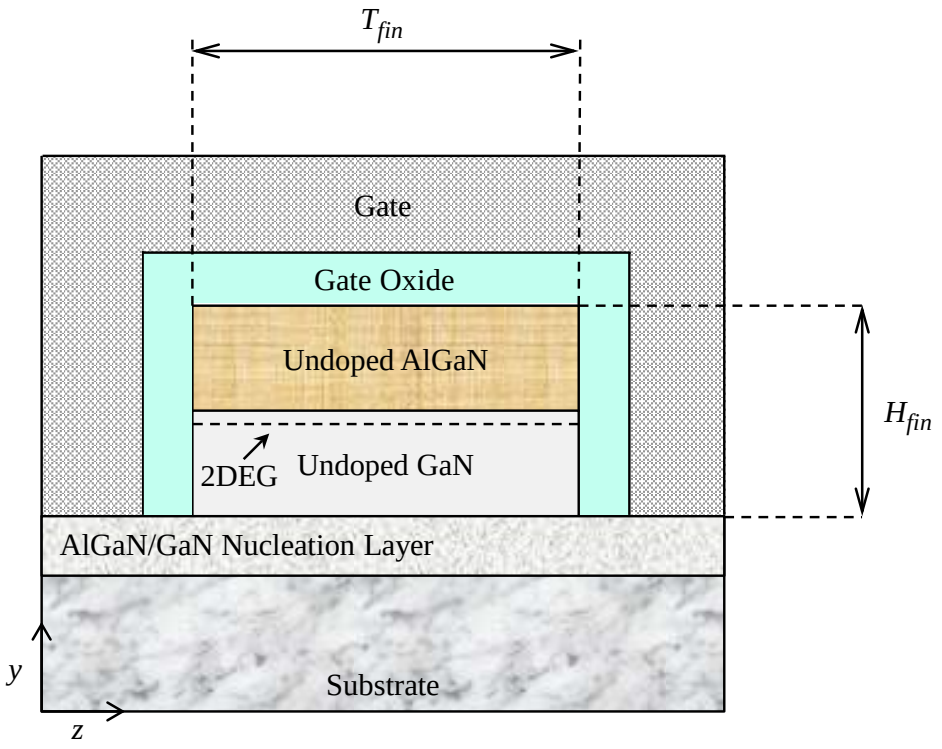

FIGURE 1.3: Typical AlGaN/GaN FinFET structure (Right View).

other hand, increasing H_{fin} reduces wafer consumption but may cause structural instability, so there is always a trade-off. As a rule of thumb, H_{fin} is usually four times less than the thickness of the fin, T_{fin} [10, 11].

1.1.1 GaN FinFETs

Semiconductor material is the basic building block of a transistor. Their main property is that their conductivity lies somewhere between insulators and conductors, and their resistance decreases when the temperature of the surroundings increase. The conductivity of a semiconductor can be controlled by changing the composition of the material (doping). The characteristics of electronic devices fabricated using semiconductors are limited by the nature of the material.

Earlier, devices were fabricated using Silicon (Si) and Germanium (Ge). They were the 1st generation of semiconductors [12]. These are also referred to as narrow bandgap semiconductors. Si has an indirect bandgap, while Ge has a direct

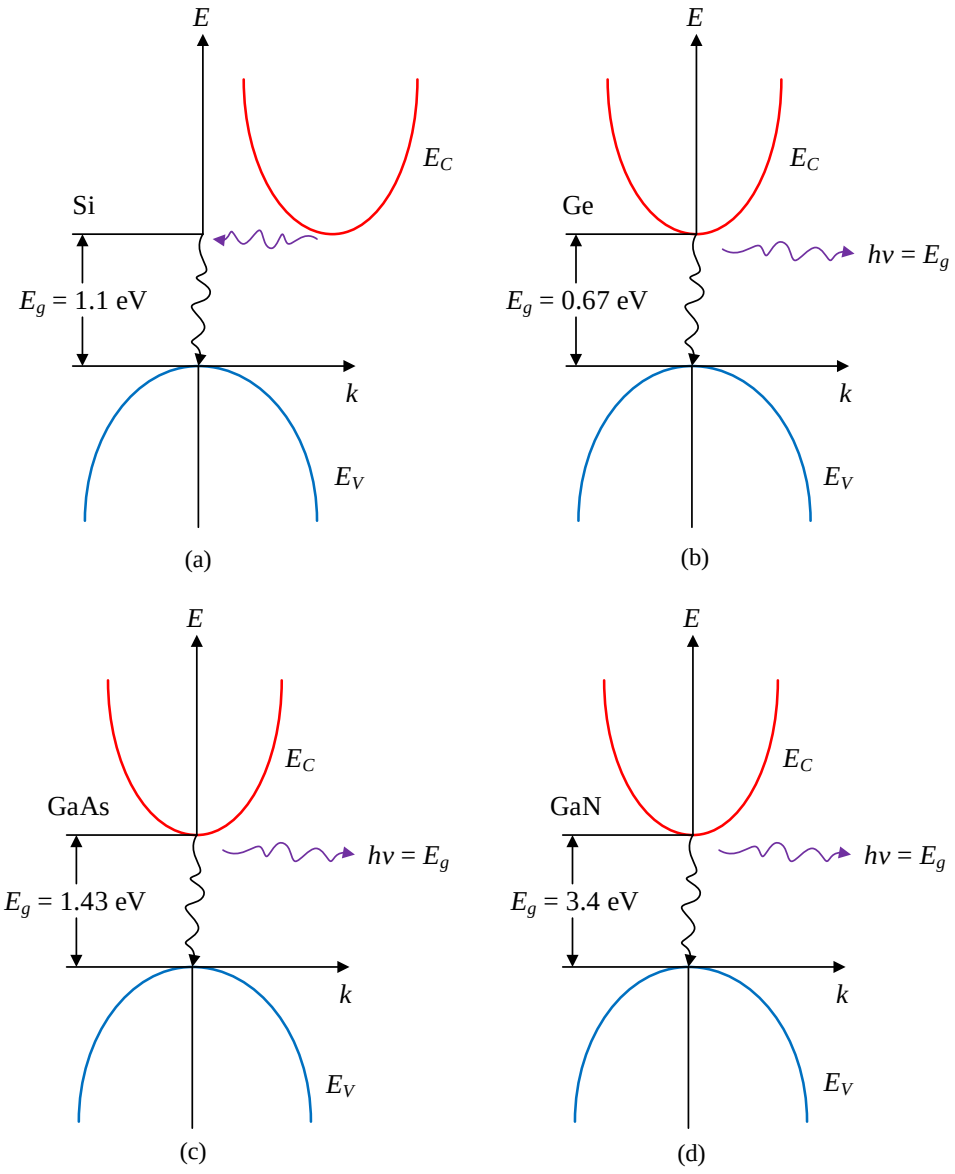

FIGURE 1.4: Direct and indirect energy bandgap diagrams of different semiconductor materials; a) Silicon, Si b) Germanium, Ge c) Gallium Arsenide, GaAs and d) Gallium Nitride, GaN.

bandgap of 1.1 eV and 0.67 eV, respectively as illustrated in Fig. 1.4. As the ambient temperature increases, the electrical properties of these materials degrade and as a result, their use is limited to moderate environments as they fail in harsh conditions.

To meet the requirements of the electronic industry, compound semiconductor materials were considered, which offered better mobility and drift velocity, called as 2nd generation semiconductors. Gallium arsenide (GaAs) was thus, grown and

TABLE 1.1: Material dependent properties of different semiconductors [16].

Parameter	Unit	Si	GaAs	Diamond	SiC	GaN
Energy bandgap	eV	1.12	1.43	5.45	3.2	3.4
Relative dielectric	-	11.9	12.5	5.5	10.0	9.5
Electron mobility	cm^2/Vs	1500	8500	2200	700	900
Thermal conductivity	W/Kcm	1.5	0.54	22	4	1.3
Breakdown field	MV/cm	0.3	0.4	10000	3.5	3.3
Saturated velocity	10^7 cm/s	1	1	1	2	2.5
Maximum temperature	°C	300	300	2100	600	700

it was found that the bandgap of the compound material was 1.43 eV (Fig. 1.4) [13]. This was better than the previous generation but still, the semiconductor had a narrow bandgap. This was not enough to meet the growing requirements of the industry to perform in high temperature based applications and thus, their use stalled.

3^{rd} generation semiconductors were introduced to cater the harsh environment applications. They have a wide bandgap (> 3 eV), which facilitates the device to perform adequately at higher temperatures. Moreover, the electrical properties of 3^{rd} generation semiconductors such as silicon carbide (SiC) and GaN at temperature > 500°C remained intact and the devices fabricated using these materials have outperformed previous generations' semiconductor devices [14, 15].

Wide band gap materials are taking over the electronic industry gradually. Their superior material properties allow them to operate in conditions where other narrow band devices fail. Since, wide band gap devices can operate at higher temperatures, that also means that they can handle higher power under normal conditions. The electric field density, which a wide band gap material device can withstand is also higher compared to a narrow band gap material device and as a result, they can be operated at much higher currents and voltages. GaN has a band gap of 3.4 eV [17] as shown in Fig. 1.4 and falls comfortably in the definition of wide band gap semiconductors. Devices fabricated using GaN have high electron mobility and velocity, which facilitate in high RF performance; high intrinsic carrier

concentration and thermal conductivity, which make the device suitable for high power and temperature related applications.

A comparison of GaN with other conventional semiconductor materials is given in Table 1.1. By studying the data of the table, it is clear that GaN based devices would be better than other semiconductor devices due to their abilities to perform at high frequency and power related applications. Moreover, intrinsic carrier concentration, n_i of GaN is 5 times less than that of other commonly used semiconductors [18, 19] as shown in Fig. 1.5. As the temperature increases, more and more electron-holes pairs are produced and they are contributing into the channel current. A very high number of electron-hole pair production can lead to device breakdown, because of uncontrolled flow of channel current. As, GaN offers low n_i at high temperatures: this allows GaN to operate under intense operating conditions. A further improvement in FinFET breakdown is reported by modifying the layer structure of the device as AlGaN/GaN FinFET, which along with higher breakdown voltages also gives higher saturation current than the conventional GaN FinFET. Moreover, the RF performance of the device is also enhanced in the case of AlGaN/GaN FinFETs. Thus, AlGaN/GaN FinFETs have become a benchmark for their superior electrical properties both at low and high power applications.

1.1.2 AlGaN/GaN FinFET Structure

Apart from the substrate, the structure of a FinFET is divided into different distinct layers and each layer has a specific function to perform. Following are the details of the AlGaN/GaN FinFET structure:

1.1.2.1 Substrate

The most robust part of the device is the substrate and it is the foundation upon which the entire device is built. It is an important factor in cost determination

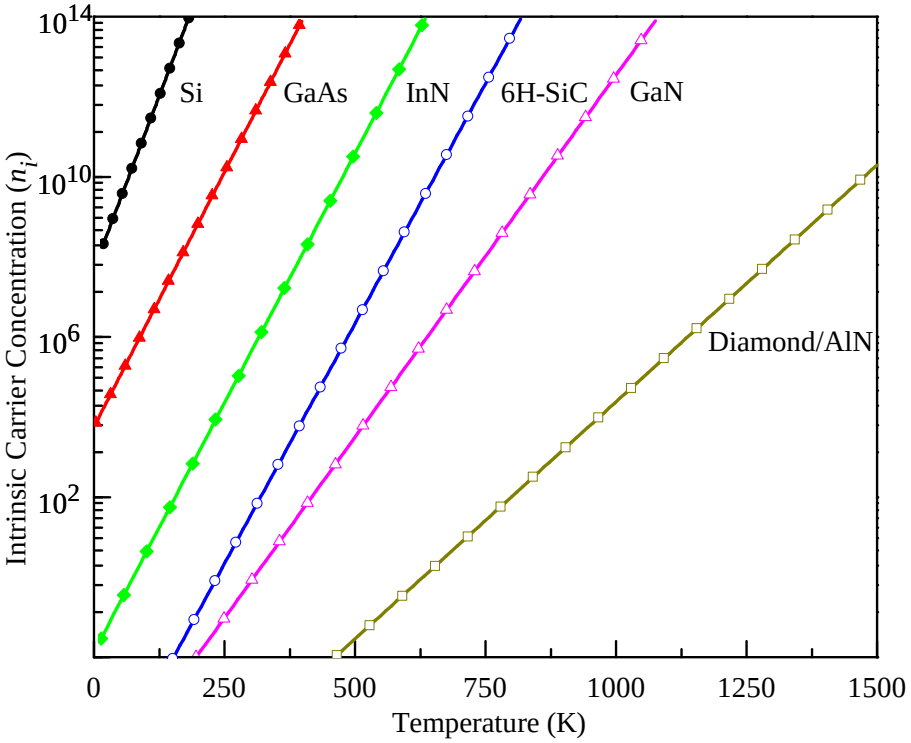

FIGURE 1.5: Intrinsic carrier concentration as a function of temperature of commonly used semiconductor materials [20].

of the device. The thickness of the substrate varies from application to application. A substrate is either a semi-insulator or a semiconductor, and is usually grown through bulk growth techniques. Si, SiC, sapphire, GaAs are commonly used substrate materials. Relative to GaN, Si offers -17% mismatch, SiC offers +3.5% while sapphire offers -16% substrate mismatch [21]. SiC is thus, a preferred substrate as it offers minimal substrate mismatch compared to other commonly used substrate materials.

1.1.2.2 Nucleation Layer

Nucleation layer is added onto the substrate through some epitaxial growth technique, such as Metal Organic Vapor Phase Epitaxy (MOCVD) or Molecular Beam Epitaxy (MBE) to improve the quality of the grown layers by reducing the lattice mismatch between the two non-native materials. It reduces the stress of the grown layers and provides a foundation for a high quality channel, which in return reduces the leakage current during the operation of the device.

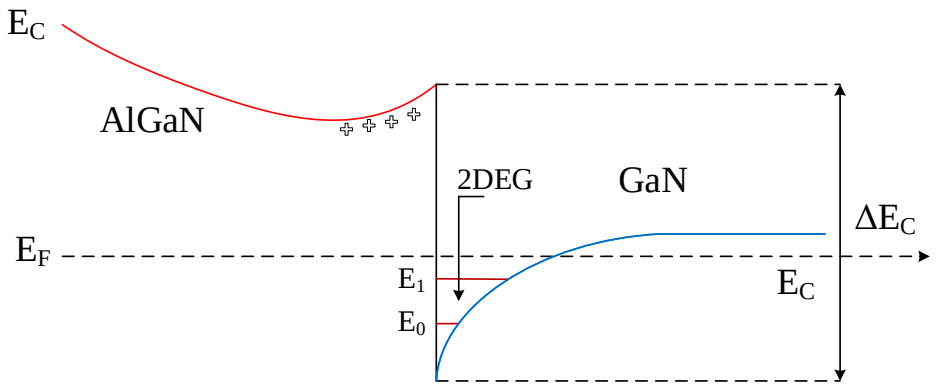

FIGURE 1.6: Difference in the bandgap energy of AlGaN and GaN resulting in the formation of 2DEG.

1.1.2.3 Carrier Layer

An undoped carrier layer is added on top of the nucleation layer as shown in Fig. 1.2. MOCVD or MBE techniques are used and special attention is given to have a high quality carrier layer such that there are almost no defects in the lattice structure. The material of the carrier layer (GaN) is chosen such that it should have band gap less than the band gap of the barrier layer (AlGaN). This results into the creation of 2 dimensional electron gas (2DEG) at the interface of the carrier and barrier layer as shown in Fig. 1.6.

1.1.2.4 Barrier Layer

Barrier layer is added on top of the carrier layer as shown in Fig. 1.2, and the band gap of the layer is greater than the carrier layer to achieve the formation of 2DEG. This layer holds Schottky metal gate therefore, its thickness is very crucial for the appropriate operation of the finished device. A slight variation in its thickness can result into the formation of a parasitic FET or completely pinched channel. It is designed in such a way that at zero gate potential, it is fully depleted and the drain to source current is only because of the 2DEG electrons.

1.1.2.5 Contact Layer

It is a heavily doped ($\sim 10^{18}$ cm^{-3}) thin layer grown on top of barrier layer to reduce the contact resistance. It is there to facilitate movement of the carriers with minimal voltage loss. It also increases the linearity of the semiconductor device for its communication to the exterior world.

1.1.3 AlGaN/GaN FinFET 2DEG

2DEG is formed by the electrons trapped in a quantum well generated by the combination of two layers having different band gaps. Electron gas refers to the confinement of free electrons in the semiconductor having length and width but almost zero thickness. Thus, the third dimension can be ignored. In Fig. 1.3, 2DEG is formed at the interface of AlGaN and GaN layers. The layers confining the 2DEG are made relatively thicker to achieve both trapping of electrons and isolation at the same time. These layers are usually undoped thus, avoiding unnecessary scattering of electrons. Therefore, electrons in 2DEG have a relatively higher mobility than other FET devices.

1.2 AlGaN/GaN FinFET Operation

FinFET is a voltage controlled current device. The output current is manipulated by changing the applied potential to the device. Potential is applied to the gate and drain terminals of the device as given in Fig. 1.2. Drain to source voltage, V_{ds} is applied to the drain-source terminal, while gate to source voltage, V_{gs} is applied to the gate-source terminal of the device.

The operation of an AlGaN/GaN FinFET is the same as of a conventional HEMT. Figure 1.7 shows the current-voltage ($I-V$) operation of an AlGaN/GaN FinFET. Initially, when V_{ds} is applied, the carriers of the 2DEG start drifting under the applied potential and current is produced. This current is proportional to the

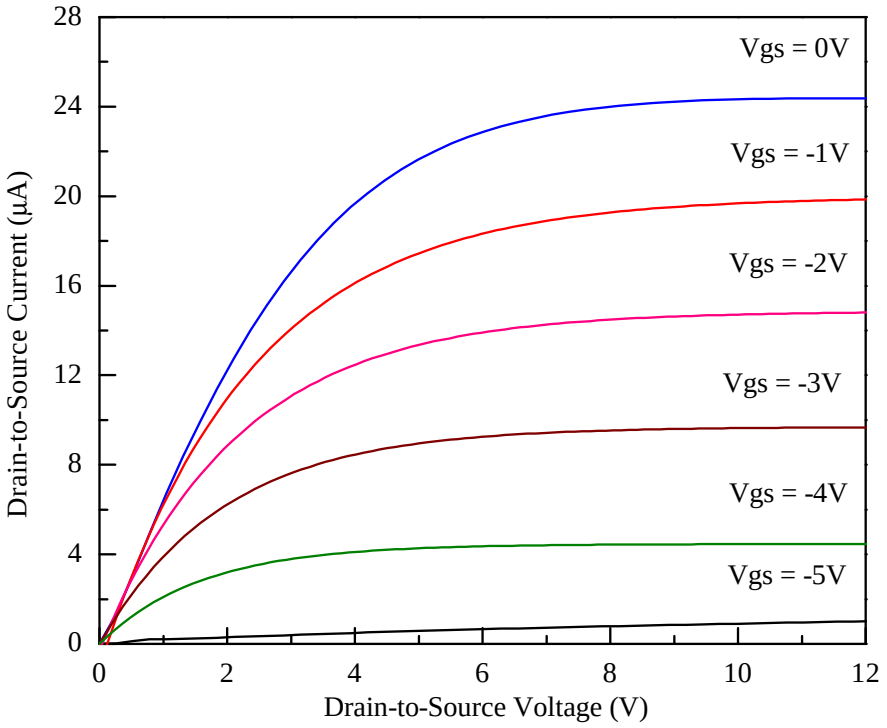

FIGURE 1.7: A typical $I-V$ characteristics curve of an AlGaN/GaN FinFET.

applied V_{ds} of the device and at this instant, the carriers are drifting with velocity, v_d less than the saturation velocity, v_{sat} of carriers. By increasing the magnitude of V_{ds}, a voltage comes after, which increasing the potential does not effect the current of the device. This potential is known as saturation voltage, $V_{ds(sat)}$. Once $V_{ds(sat)}$ is achieved, carrier velocity becomes $v_d = v_{sat}$ and further increase in V_{ds} will not increase the drain to source current, I_{ds}. Changing V_{gs}, on the other hand, changes the 3D depletion height of the channel. A negative increase in V_{gs} reduces I_{ds} of a FinFET. When V_{gs} reaches threshold potential, V_{th}, then I_{ds} reduces to a negligible value and the device is pinched off.

1.3 DC Performance

The introduction of FinFETs has opened exciting new doors for integrated circuits (ICs). Their relatively small gate lengths allow compact packing of FinFETs in integrated circuit design, which results into less wafer consumption per transistor.

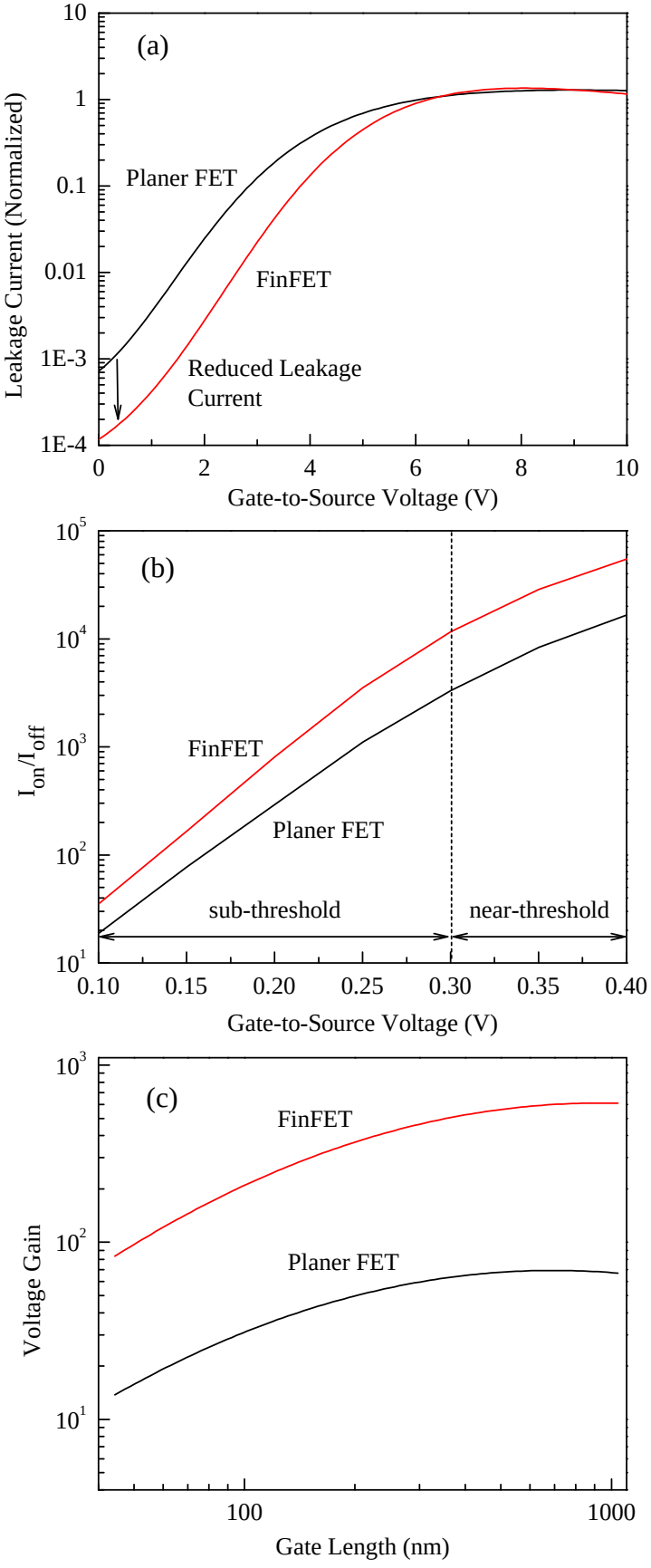

FIGURE 1.8: DC performance of FinFET compared with planer FET.

This is a reason that more and more FinFETs are being adopted into IC fabrication. FinFETs ability to operate under low voltage conditions; results in a low V_{th}, therefore, there is minimum battery consumption in the off state. On the other hand, the drive current per unit area of FinFETs is considerably high, which can be further improved by varying the number of fins of the transistor.

FinFETs offer stable saturation current as the gate has more control over the device as shown in Fig. 1.7. As the $I - V$ curves in saturation region are much more flatter, there is low dynamic power consumption. The tri-gate structure fully depletes the channel thus, better on and off contrast due to a fully depleted structure is achieved. In conventional FETs, leakage current consumes a large portion of power. This waste of power is reduced by using a FinFET device [22, 23]. Figure 1.8(a) shows a comparison between the normalized leakage current and applied V_{gs} for both planer FETs and FinFETs. At higher gate bais, both planer and fin FETs show the same amount of gate leakage. But at low values of V_{gs}, there is a considerable decrease in leakage current observed in FinFETs. This could be associated to the tri-gate structure of the device where, the gate has more control, reducing the leakage of the current.

Figure 1.8(b) compares the ratio of on current, I_{on} to the off current, I_{off}. This ratio is a measure of the quality of the device. The higher the ratio, higher is the device output current while at the same time, the leakage current is minimum. As evident from the figure, in both sub-threshold and near-threshold voltages, FinFETs outperform conventional FETs. In Fig. 1.8(c), a correlation between the voltage gain and the gate length of both planer and fin FETs is given. Examining the figure, it is observed that FinFETs offer higher voltage gain across the varying gate lengths. This implies that such devices will exhibit improved RF performance and the detail of which is given in the following section.

1.4 RF Performance

Gate length, L_g plays an important role in determining the RF performance of a FET. AlGaN/GaN FinFETs have a great potential to compete for electronic devices meant for AC applications, because of their superior electrical properties. When a high frequency AC signal is applied at the gate of a FET, its Miller capacitors come into play as they couple the RF signal with the device and determine its maximum frequency of operation.

Miller capacitors namely: gate to source capacitor, C_{gs} and gate to drain capacitor, C_{gd} are crucial in determining the transit time, τ of the device, which translates the time taken by the device to respond to an incoming changing signal. τ is directly determined by the L_g of the device. FinFETs by their very design can have a relatively small L_g, which allows the device to have a smaller τ and hence, a faster response time. Figure 1.9(a) shows the difference of τ for both planer and fin FETs [23]. It can be seen that at operating voltage of 1 V, 18% improvement in τ is observed while at 0.7 V, the improvement is increased by 37% and the trend of improvement is consistent throughout the graph. This solidifies the position of FinFETs in the field of high frequency analog electronics.

Figure 1.9(b) shows that by varying L_g, the output conductance, g_d of FinFETs compared to other conventional FETs is lower [24]. This could again be due to the tri-gate structure of the device. Moreover, the voltage gain, given in Fig. 1.8(c), which is a ratio of transconductance to output conductance is higher due to low g_d, which increases the RF performance of FinFETs. Figure 1.9(c) also describes the effect of L_g on the cut-off frequency, f_c of both fin and planer FETs. As observed from the graph, FinFET offers a large f_c, which once again supports the claim that FinFETs have superior RF performance relative to their planer single gate FET counterparts.

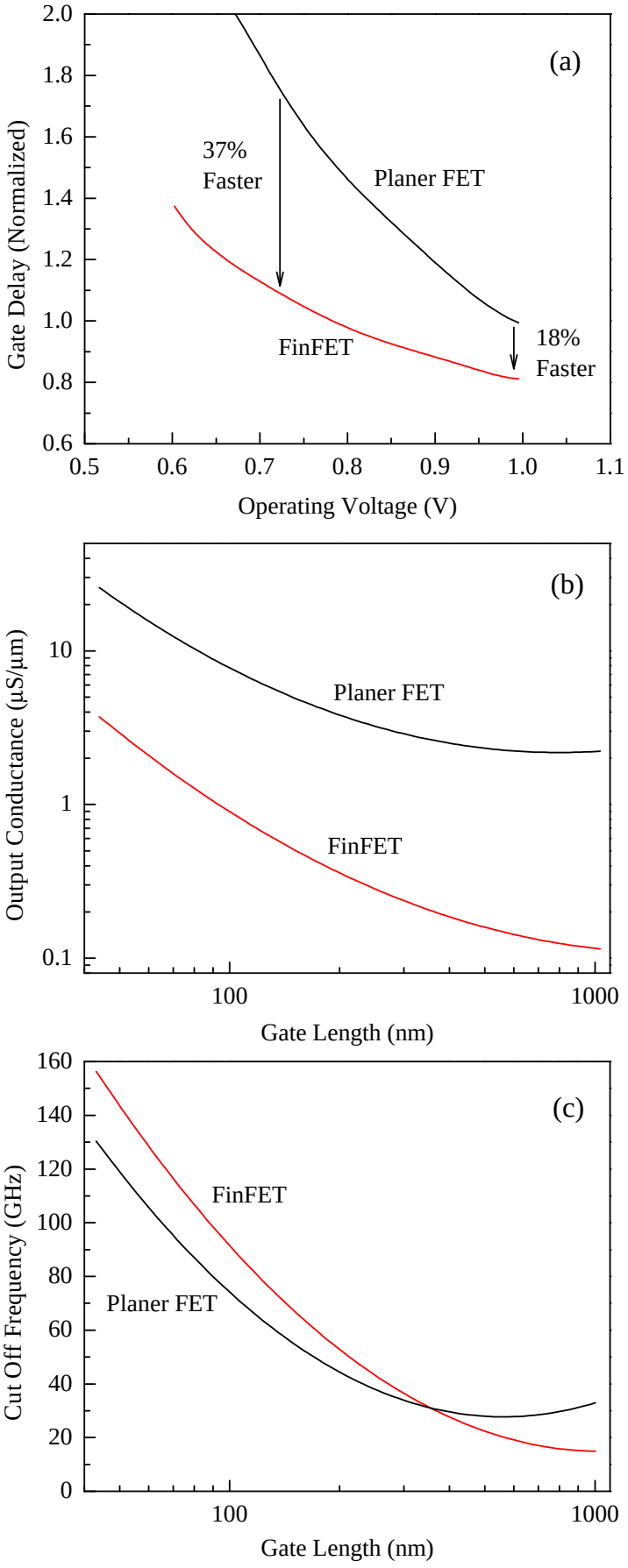

FIGURE 1.9: RF performance of FinFET compared with planer FET.

1.5 Summary

This chapter presents an overview of AlGaN/GaN FinFETs as a potential candidate for both power and microwave applications. A detailed discussion is given why FinFETs are becoming popular for microwave and power related circuitries. By employing AlGaN/GaN heterostructure as the basic material for the device, FinFETs have the potential for operation in harsh environments and tense operating conditions. The tri-gate structure of the device offers more control and allows full depletion of the channel and as a result, FinFETs experience less leakage current and dynamic power loss. A description pertaining to the functioning of the device is presented in an attempt to realize its operation and electrical response both at DC and AC level. It has been shown that GaN based FinFETs have a great future in high frequency analogue electronic circuitries.

Chapter 2

Literature Review

2.1 Introduction

Ever since the inception of CMOS devices, the issue of scalability remained a pressing concern for the design engineers [25–27]. As the size of the devices shrunk, parasitic effects were observed. These effects hindered the possibility of further device shrinkage and the gate of the devices began to lose control [28–30]. As the size of the transistor is directly proportional to the short channel effects (SCE), therefore, a decrease in gate length below 20 nm is completely impractical [31]. To overcome these effects and increase the controllability of gate, multi-gate FETs were introduced.

Multi-gate FETs are the alternative to planer FETs, as they have more than one gate which acts on the device channel. This induces more control on the device and helps in reduction of SCEs [32, 33]. FinFET is one type of multi-gate FET. FinFETs provide reduced parasitic capacitance, but the trade off is that their fabrication technology is complex [34]. They also consume less power, are easily scalable and relatively immune to SCEs [35]. The following sections will explore in detail, FinFET technology, its applications and its challenges.

2.2 FinFET Technology

In 1990, Hisamoto et al. [8] presented a fin like transistor. They named it DELTA. It was observed that due to the multi-gate structure, the control of the gate on the channel was enhanced and also, the SCEs were reduced. Huang et al. [36] developed a 18 nm *p*-channel FinFET and showed that the tri-gate geometry is effective in reducing the SCEs. Hisamoto et al. [6] also reported reduced SCEs with 17 nm double gate FinFET. Huang et al. [9] observed that below 50 nm regime, double gate FinFETs have excellent short channel behavior and they showed promise in scaling the existing CMOS technology beyond the 50 nm mark.

Yu et al. [37] reported the characteristics of a double gate 10 nm FinFET. They observed that the SCEs of the transistor reduced significantly compared to conventional MOSFETs. Xuan et al. [38] developed flash memory from 40 nm FinFET. They reported excellent read/write characteristics along with long retention time and endurance. Yang et al. [39] reported an ultra scaled nano wire FinFET. They reduced the gate length to 5 nm and reported a reduced gate delay and low leakage current. Lederer et al. [40] reported the effect of fin width on the AC performance of the device. They showed that by decreasing the fin width, FinFETs have the potential to operate above 250 GHz. Kaneko et al. [41] reported low parasitic resistance and high performance with dopant segregated Schottky drain/source 15 nm FinFET.

Baravelli et al. [42] studied the effect of line edge roughness on the performance of FinFETs. They showed that line edge roughness degrades the electrical performance of FinFETs however, at lower doping its effects are minimized. Poljak et al. [43] studied the effect of silicon on insulator (SOI) on FinFETs characteristics. They concluded that SOI FinFETs offer better sub-threshold and on state performance. Also, the drive current of SOI based FinFETs is relatively better. In 2009, Poljak et al. [44] reported that at lower doping and reduced drain/source junction depth relative to the gate bottom, bulk FinFETs performance becomes equal or greater than SOI FinFETs with no increase in the complexity of the device. Chiarella et al. [45] reported that by having lightly doped fins and SOI substrates,

V_{th} mismatch and junction capacitance can be reduced and also, higher mobility and voltage gain can be obtained. Saini et al. [46] reported that when the gate length to fin thickness reaches below 1.5, severe SCEs are observed in FinFETs. Increasing the fin height increases the drive current but it also destabilizes the device and generates SCEs.

Saremi et al. [47] reported that by using ground plane, drain induced barrier lowering was reduced. Also, by using the ground plane technology, the leakage current was significantly reduced. Nandi et al. [48] studied the effect of dual gate spacer layer on the power consumption of both $n-$ and $p-$type FinFETs. They concluded that by adding the dual gate spacer layer, less battery consumption is observed. Gaynor et al. [49] studied the effect of fin shape on the leakage current of the device. They showed that triangular fin shape reduces the leakage current to about 70% relative to a complete rectangular fin. Mohapatra et al. [50] studied the effect of fin thickness and height on the RF performance of FinFETs. It was observed that narrower fins provided good immunity towards SCEs while taller fins increased the drive current of the device.

Karl et al. [51] developed an 84 Mb static random access memory (SRAM) using 14 nm FinFETs, which can operate at 1.5 GHz by using a 0.6 V potential. The read/write of the SRAM was controlled by capacitive charge share and a 24% reduction in the write energy was observed. Song et al. [52] developed an SRAM using 10 nm FinFETs. They reported improved transient time and read/write margins. Singh et al. [53] developed a 14 nm FinFET for RF and analog applications. They observed that f_{max} of the devices were 227 GHz along with low noise, high gain and high breakdown voltage, and proved suitability of their devices for 5G mobile communication systems. Chhabra et al. [54] developed a junctionless GaAs FinFET device for biological sensing. They used hafnium oxide (HfO_2) as the oxide material and found that the switching speed of the device increases by three times as that of a conventional CMOS device. Furthermore, the efficiency and sensitivity of the FinFET was improved and a reduction in noise figure was also claimed. A summary of FinFET technology discussed in the preceding paragraphs is presented in Table 2.1.

TABLE 2.1: A brief overview of FinFET technology.

Year	Author	Description	Ref.
1990	Hisamoto et al.	First multi-gate transistor	[8]
1999	Huang et al.	18 nm *p*-channel tri-gate FinFET	[36]
2000	Maruska et al.	Reduced SCEs in 17 nm double gate FinFET	[6]
2001	Huang et al.	FinFET past 50 nm regime	[9]
2002	Yu et al.	10 nm double gate FinFET	[37]
2003	Xuan et al.	40 nm flash memory	[38]
2004	Yang et al.	Nano wire 5 nm FinFET	[39]
2005	Lederer et al.	FinFETs design to operate above 250 GHz	[40]
2006	Kaneko et al.	High performance 15 nm FinFET	[41]
2007	Baravelli et al.	Edge roughness and FinFET performance	[42]
2008	Poljak et al.	SOI FinFETs sub-threshold characteristics	[43]
2009	Poljak et al.	Low doped bulk FinFETs performance	[44]
2010	Chiarella et al.	Low doped FinFETs performance	[45]
2011	Saini at al.	Effect of fin dimension on performance	[46]
2012	Saremi et al.	Fabrication using ground place concept	[47]
2013	Nandi et al.	FinFET with dual k-spacer layer	[48]
2014	Gaynor et al.	Effect of fin width on performance	[49]
2015	Mohapatra et al.	Effect of fin shape on performance	[50]
2016	Karl et al.	84 Mb, 0.6 V SRAM using FinFETs	[51]
2017	Song et al.	10 nm FinFET SRAM	[52]
2018	Singh et al.	14 nm FinFET for RF applications	[53]
2019	Chhabra et al.	Junctionless GaAs FinFETs	[54]

2.3 FinFET Models

To understand the device behavior in more detail, device models are required. In 2001 Chen et al. [55] presented a potential model for double gate FinFET in which 1D Poisson equation was solved to get the potential distribution inside the channel. Enfeng et al. [56] simulated the characteristics of SOI FinFETs using a Quasi-3D numerical model. Chen et al. [57] developed a double gate threshold model for short channel FinFETs. They solved 2D Poisson equation to find the potential distribution and by using channel potential, they evaluated V_{th}. Rehman [58] proposed an $I-V$ model for tri-gate FinFETs, which predicted the device characteristics once the inversion layer is created between the drain and source of the device.

Lin et al. [59] presented a model for independent gate FinFETs, which was developed by solving Poisson equation in 2D for both the gates independently. Simt et al. [60] proposed a DC model for tri-gate FinFETs, which was developed by solving 1D Poisson equation for potential evaluation followed by the assessment of charge accumulation between drain and source terminals. Crupi et al. [61] presented a non-linear $I-V$ model for tri-gate FinFETs, which was derived with the help of lookup tables. Gu et al. [62] proposed a leakage current model for double gate FinFET devices. Their model involved minimum physics, rather it was developed using empirical equations. Crupi et al. [63] developed an analytical approach to extract AC parameters of FinFETs.

Crupi et al. [64] also presented a non-linear RF model for Si FinFETs. They use de-embedding techniques to assess parasitic capacitance of the device. Yesayan et al. [65] developed a physics based model for lightly doped Si FinFETs. They also added quantum mechanical effects in their model. Fasarakis et al. [66] proposed a compact physics based model for short channel FinFETs. They added the effect of channel length modulation on the device $I-V$ characteristics. Ko et al. [67] solved 3D Poisson equation numerically to find the effect of gate length on SCEs of tri-gate FinFETs. Chen et al. [68] developed a 3D numerical model to assess the effect of temperature on the channel resistance of the device.

TABLE 2.2: A brief overview of FinFET models reported in the literature.

Year	Author	Description	Ref.
2001	Chen at al.	1D Poisson potential model	[55]
2002	Enfeng et al.	Quasi-3D numerical model	[56]
2003	Chen at al.	Threshold voltage model	[57]
2004	Rehman	Tri-gate FinFET $I-V$ model	[58]
2005	Lin et al.	Independent gate FinFET model	[59]
2006	Simt et al.	1D Poisson $I-V$ model	[60]
2007	Crupi et al.	Non-linear model with lookup tables	[61]
2008	Gu et al.	Leakage current model	[62]
2009	Crupi at al.	Non-linear AC model	[63]
2010	Crupi et al.	Parasitic capacitance model	[64]
2011	Yesayan et al.	Physics based model for lightly doped FinFETs	[65]
2012	Fasarakis et al.	Short channel effects model	[66]
2013	Ko et al.	3D Poisson numerical model for SCEs	[67]
2014	Chen et al.	FinFET thermal model	[68]
2015	Duarte et al.	Double gate analytical $I-V$ model	[69]
2016	Aziz et al.	Physics based SPICE model	[70]
2017	Yu et al.	Parasitic resistance model	[71]
2018	Mei et al.	Monte Carlo model for leakage current	[72]
2019	Das et al.	Cylindrical FinFET model	[73]

Duarte et al. [69] presented an $I-V$ model for double gate FinFETs by finding the charges at the drain and source terminals using a 2D Poisson equation. Aziz et al. [70] presented a physics based SPICE model for FinFETs. They considered depolarization field due to non ideal contacts. Yu et al. [71] modeled hot carrier based degradation of FinFETs by considering self-heating effects. Mei et al. [72] used Monte Carlo method to find parasitic resistance of FinFETs associated with leakage current. Das et al. [73] presented a 2D Poisson equation based analytical model for cylindrical FinFETs and established the credibility of the model by comparing the results to TCAD simulations. For quick visualization, a summary of the discussed FinFET models is presented in Table 2.2.

2.4 Device Challenges

Moving from conventional 2D FET to 3D FinFETs possess many fabrication challenges which could seriously hamper the device performance if not catered adequately; some of which are highlighted below:

2.4.1 Fin Shape

The shape of the fin determines the overall performance of the device. The SCEs degrade due to the slant of the fin. However, a slanted fin leads to the current crowding and thus, deteriorates the overall performance of the device [74]. FinFETs with lower height are not effected by the angle of the fin but, as the height of the fin increases, fin angle must increase and for optimum performance, it should be perpendicular [75].

2.4.2 Fin Thickness and Height

As the thickness of the fin reduces, less SCEs are observed [76, 77]. As a result V_{th} and sub-threshold swing also reduces. The same effect of V_{th} and sub-threshold

swing is observed with fin height. The width of the device translates into both height and thickness of the fin. Due to the fabrication limitations, the effective width of the device is always a multiple of fin thickness and height. Therefore, variation in fin width is always quantized [78].

2.4.3 Fin Doping

FinFETs are preferred to be undoped, however to improve V_{th} and reduce leakage current lightly doped FinFETs are adopted [1]. The drain and source terminals of FinFETs must be heavily doped to reduce the series resistance of the device. To reduce the parasitic series resistance, epitaxial growth is carried out which is retained on the drain and source regions of the device, and the same is removed from the fin to minimize gate leakage [79].

2.4.4 Parasitic Capacitance

Due to more overlap area across the back and front gate, the capacitance of the device increases. This in turn decreases the RF performance of the device. Fin height can be varied to control the effect of parasitic capacitance. By increasing the fin height, and decreasing the fin slant, parasitic capacitance can be reduced [80, 81].

2.5 Circuit Challenges

As FinFET is a 3D device, fabrication process is much more complex than ordinary planer FETs. On the other hand, it is necessary for all the fins present in the circuit to have the same height in order to maintain uniform performance of each device. Due to the limitation of the fabrication process, variation from device to device is inevitable. This imposes a challenge for FinFETs which ought to be integrated

in large circuitries. Following are some of the challenges faced by FinFETs in the electronic industry:

2.5.1 Integration

In FinFET technology, the margin of error is significantly less. For a device of <20 nm, the variation in the fin width must be <1 nm to ensure optimum performance and low V_{th} [75]. Therefore, the separation between the device must follow a strict rule. Due to the ultra confined geometry of the FinFET circuits, they are prone to self-heating effects which could degrade their performance significantly [82].

2.5.2 SRAM

Due to the growing speed requirement of the electronic circuitries, down scaling of SRAMs was essential. FinFETs provided the solution for down scaling due to their unique structure and relative immunity to SCEs. Many types of FinFETs are utilized in the production of SRAMs, namely: Junctionless FinFETs [83], Pseudo spin FinFET [84], Tunnel FinFET [85], etc. By using Junctionless FinFETs, higher on current is obtained but the circuit becomes more complex [86]. To minimize power consumption in SRAMs, undoped FinFETs with Hi-k spacer layer is used [87]. Tunnel FinFETs allow the scaling of the supply voltage without increasing the static power to the SRAM [84].

2.5.3 Voltage Transfer Characteristics

The slope of voltage transfer characteristics is steeper in FinFET inverters compared to conventional CMOS inverters. At equal drive strength, FinFET technology shows superiority over COMS based circuits [88]. However, when we move towards complex circuits, such as NAND or NOR gates, it is very difficult to match the derive strength due to the discrete device width, which is determined by the number of fins.

2.5.4 Flash Memory

FinFET based flash memory devices are exceptional in reducing the SCEs observed in conventional memories. They also have high read/write currents and punch-through margins [37, 89, 90]. Many types of flash memories made from FinFETs are reported in the literature. Silicon oxide nitride oxide silicon (SONOS) based flash memory, bandgap engineered SONOS and FinFET floating-gate memory are some of the promising technologies [90, 91]. Due to low gate-coupling ratio and large fin thickness, floating-gate FinFET memory is prone to gate interference between adjacent memory cells. SONOS memory is immune against this effect but has low erase speed and memory retention while SONOS memory which has high engineered bandgap show great promise for both of these problems [91].

2.6 Research Gaps

As FinFET is a 3D device, its modeling techniques differ from that of conventional planer FETs. Based on the literature review, both from the device as well as from modeling perspective, following research gaps have been identified:

1. In FinFET devices, fin height plays an important role in determining the device characteristics. For relatively high fin devices, z directed field could play an important role in determining the overall electrical characteristics of the device. This requires a 3D model, which should include the effect of height in assessing the DC characteristics of FinFETs.

2. As FinFETs can have independent gates acting on the same channel, an analytical model, which can predict the response of such devices by incorporating the effect of channel height on the device DC characteristics would be beneficial for design engineers.

3. Conventional FinFET models work on the principle of bulk and intrinsic charge concentrations and not on sheet charge density thus, they are prone

to produce error in predicting the characteristics of AlGaN/GaN based FinFETs. Therefore, there is a need to develop a model which can assess the $I-V$ characteristics of AlGaN/GaN FinFETs by considering the effect of side gates on the 2DEG.

4. A heavy mathematical based analytical model is usually difficult to implement from a design engineer perspective. Thus, there is a need to develop a simple model, which links the device physical parameters with its characteristics to a good degree of accuracy. Such a model would be a useful tool for CAD related applications.

2.7 Summary

In this chapter, a thorough literature review of FinFET technology is presented. In has been shown that the characteristics of FinFETs depend upon the geometry of the device. It has also been established that FinFETs offer better control upon short channel effects, compared to conventional FET devices. Numerous models available in the literature for FinFETs characteristics are presented and their limitations have been discussed. The challenges faced by FinFET technology, both at device and circuit level have been highlighted and in light of those, research gaps have been identified.

Chapter 3

A 3D Analytical Model for FinFETs DC Characteristics

3.1 Introduction

To enhance the electrical properties of FETs and to achieve large scale integration, double gate FETs [92], tunnel FETs [93] and FinFETs [94] have been proposed. A FinFET device has a fin shaped channel enveloped by a 3D gate. This provides a 3D gate control upon the channel, resulting in improved device characteristics. Thus, a FinFET, relative to conventional FETs, is a 3D device, which offers better gate-control and low off-state leakage current [95].

As size of the FinFETs is shrinking rapidly, this posed a greater challenge on the design engineer to develop a model which can predict the device characteristics to an acceptable accuracy. A comprehensive model allows the design engineer to study the effect of a device physical parameters on its characteristics and provides an improved device understanding.

Numerous models explaining the fundamental working principle of FinFETs have been developed by various researchers working in the field. Yesayan et al. [65] presented a physics based model for submicron FinFETs. The model was developed for Si based FinFETs with lightly doped body. They tested their model with

3D numerical solutions of the device but the model was not validated through experimental data.

Ghosh et al. [96] presented a drain current model for cylindrical and surrounded metal oxide semiconductor FinFETs. They incorporated drain induced barrier lowering in their model. But the model was not judged on real world devices. Fsarakis et al. [66] also proposed a drain current model for FinFETs. Their model was designed for lightly doped FinFETs and they also considered short channel effects caused by the scaling of the device.

Paydavosi et al. [97] presented a surface potential based model for multi-gate FinFETs. 2D Poisson equation was solved to find the potential distribution inside the channel. $I-V$ characteristics were then evaluated using the solution of the Poisson equation. The model also included real device data and short channel effects. Duarte et al. [98, 99] presented a drain current model for multi-gate FinFETs by using arbitrary potential method. Their model incorporated both sub-threshold inversion and finite doping density in the channel. They showed that their model is computationally efficient and can be used reliably in multi-gate FinFET simulators.

Kumari et al. [100] studied the effect of gate underlap on the performance of FinFETs using a Quasi-3D analytical model. They compared their model with 3D ATLAS simulations [101]. They however, did not compare the model with experimental data. Kumar et al. [102] developed a 2D analytical model for Ring FETs and compared the results with ATLAS 3D simulations. They also studied the effect of ring parameters on the drain current of the device. However, characteristics attained from their model expressions were not compared with any experimental data, therefore, it is difficult to ascertain the accuracy of the model.

In this chapter, an analytical model for tri-gate Si FinFETs is presented. The model includes both the undoped and doped channel conditions. 3D Poisson equation is solved to find the potential distribution inside the channel. By using drift equation and the channel potential, an $I-V$ expression for FinFETs is derived. It has been shown that 3D solution of Poisson equation with appropriate

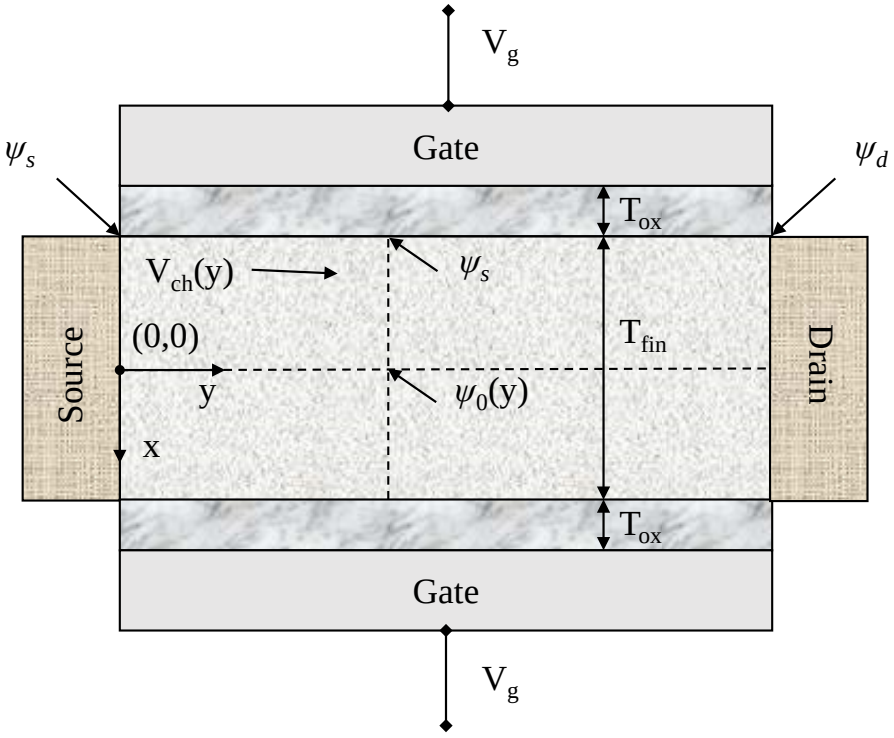

FIGURE 3.1: Crossectional view of a double gate FET.

boundary conditions generate improved $I-V$ characteristics relative to 2D models. The accuracy of the model is also checked using experimental data of devices of varying dimensions.

3.2 Model Development

3.2.1 2D Surface Potential Model

To evaluate the channel current of a FinFET, an accurate assessment of internal channel potential is required. Figure 3.1 shows crossectional view of a double gate FinFET. The potential inside the channel is the result of both inversion and bulk carriers [103]. A 2D surface potential model assumes that the applied field from both the gate electrodes, as shown in Fig. 3.1, controls the flow of the current between drain and source. This results in a simplified surface potential model, wherein, height of the fin is not taken into consideration. In this case,

the $x-$directed field dominates the y directed field and most of the current flows through the $x-y$ (Fig. 3.1) plane. Thus, for such a system, Poisson equation that includes both the inversion and bulk carriers can be expressed as

$$\frac{\partial^2\psi(x,y)}{\partial x^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi(x,y)+\phi_B-V_{ch}(y)}{V_m}\right) + \frac{qN_a}{\epsilon_{si}} \tag{3.1}$$

$V_{ch}(y)$ determines the channel potential and from Fig 3.1, $V_{ch}(0) = 0$ and $V_{ch}(L_g) = V_{ds}$. Here

$$\phi_B = V_m \ln\left(\frac{N_a}{n_i}\right) \tag{3.2}$$

and

$$V_m = \frac{k_B T}{q} \tag{3.3}$$

Eq. (3.1) can be simplified such that the term N_a can be ignored when the channel is lightly doped [104]. $\psi(x,y)$ of Eq. (3.1) can be written as

$$\psi(x,y) = \psi_1(x,y) + \psi_2(x,y) \tag{3.4}$$

where, $\psi_1(x,y)$ is the potential due to the inversion carriers and $\psi_2(x,y)$ represents the potential due to bulk carriers. Considering the inversion carriers alone, one can write

$$\frac{\partial^2\psi_1(x,y)}{\partial x^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi_1(x,y)+\phi_B-V_{ch}(y)}{V_m}\right) \tag{3.5}$$

Integrating Eq. (3.5), reveals

$$\frac{\partial\psi_1(x,y)}{\partial x} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi_1(x,y)+\phi_B-V_{ch}(y)}{V_m}\right) \times \frac{V_m}{\frac{\partial\psi_1(x,y)}{\partial x}} \tag{3.6}$$

$$\left(\frac{\partial\psi_1(x,y)}{\partial x}\right)^2 = \frac{V_m qn_i}{\epsilon_{si}} \exp\left(\frac{\psi_1(x,y)+\phi_B-V_{ch}(y)}{V_m}\right) + c_1 \tag{3.7}$$

$$\frac{\partial\psi_1(x,y)}{\partial x} = \sqrt{\frac{V_m qn_i}{\epsilon_{si}} \exp\left(\frac{\psi_1(x,y)+\phi_B-V_{ch}(y)}{V_m}\right) + c_1} \tag{3.8}$$

The boundary conditions of Eq. (3.8) are subjected to are

$$\left.\frac{\partial\psi_1(x,y)}{\partial x}\right|_{x=0} = 0 \qquad \text{and} \qquad \psi_1(x=0,y) = \psi_0(y) \tag{3.9}$$

By using Eqs. (3.8) and (3.9), the value of c_1 is evaluated as

$$c_1 = -\frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_0(y) + \phi_B - V_{ch}(y)}{V_m}\right) \tag{3.10}$$

Combining Eq. (3.8) and Eq. (3.10), one gets

$$\begin{aligned}\frac{\partial\psi_1(x,y)}{\partial x} = \Bigg(\frac{V_m q n_i}{\epsilon_{si}}\Bigg[\exp\left(\frac{\psi_1(x,y) + \phi_B - V_{ch}(y)}{V_m}\right) \\ - \exp\left(\frac{\psi_0(y) + \phi_B - V_{ch}(y)}{V_m}\right)\Bigg]\Bigg)^{1/2}\end{aligned} \tag{3.11}$$

Now, by integrating Eq. (3.11)

$$\begin{aligned}&\int \frac{\partial\psi_1(x,y)}{\sqrt{\frac{V_m q n_i}{\epsilon_{si}}\left[\exp\left(\frac{\psi_1(x,y) + \phi_B - V_{ch}(y)}{V_m}\right) - \exp\left(\frac{\psi_0(y) + \phi_B - V_{ch}(y)}{V_m}\right)\right]}} \\ &= \int \partial x\end{aligned} \tag{3.12}$$

which can also be written as

$$\begin{aligned}&\frac{\int \partial\psi_1(x,y)}{\left(\left[\sqrt{\exp\left(\frac{\psi_1(x,y) + \phi_B - V_{ch}(y)}{V_m}\right)}\right]^2 - \left[\sqrt{\exp\left(\frac{\psi_0(y) + \phi_B - V_{ch}(y)}{V_m}\right)}\right]^2\right)^{1/2}} \\ &= x\sqrt{\frac{V_m q n_i}{\epsilon_{si}}}\end{aligned} \tag{3.13}$$

To solve Eq. (3.13), substitution method is used. Let

$$\sqrt{\exp\left(\frac{\psi_1(x,y) + \phi_B - V_{ch}(y)}{V_m}\right)} = a\sec\theta \tag{3.14}$$

and,

$$\sqrt{\exp\left(\frac{\psi_0(y)+\phi_B-V_{ch}(y)}{V_m}\right)}=a \tag{3.15}$$

By taking partial differential of Eq. (3.14), one gets

$$\frac{1}{2}\left[\exp\left(\frac{\psi_1(x,y)+\phi_B-V_{ch}(y)}{V_m}\right)\right]^{-1/2}\exp\left(\frac{\psi_1(x,y)+\phi_B-V_{ch}(y)}{V_m}\right)\times\frac{\partial\psi_1(x,y)}{V_m}$$
$$=a\sec\theta\tan\theta\;\partial\theta \tag{3.16}$$

Combining Eqs. (3.14) and (3.16) reveals

$$\partial\psi_1(x,y)=2V_m\tan\theta\;\partial\theta \tag{3.17}$$

Substituting Eq. (3.14), (3.15) and (3.17) in Eq. (3.13), one gets

$$x\sqrt{\frac{V_m q n_i}{\epsilon_{si}}}=\int\frac{2V_m\tan\theta}{\sqrt{a^2\sec^2\theta-a^2}}\partial\theta \tag{3.18}$$

as $a^2\sec^2\theta-a^2=a^2\tan^2\theta$, so

$$x\sqrt{\frac{V_m q n_i}{\epsilon_{si}}}=\int\frac{2V_m\tan\theta}{a\tan\theta}\partial\theta=\frac{2V_m\theta}{a}+c_2 \tag{3.19}$$

The expression for θ can be derived from Eq. (3.14) and (3.15)

$$\sec^{-1}\left[\sqrt{\exp\left(\frac{\psi_1(x,y)-\psi_0(y)}{V_m}\right)}\right]=\theta \tag{3.20}$$

By using boundary conditions given by Eq. (3.9) along with Eq. (3.20), one can readily obtained that $c_2=0$. Now, by rearranging Eq. (3.19), one gets

$$\sqrt{\frac{qn_ia^2}{V_m\epsilon_{si}}}\times\frac{x}{2}=\theta \tag{3.21}$$

So, substituting the value of θ in Eq. (3.21)

$$\sqrt{\frac{qn_ia^2}{V_m\epsilon_{si}}} \times \frac{x}{2} = \sec^{-1}\left[\sqrt{\exp\left(\frac{\psi_1(x,y)-\psi_0(y)}{V_m}\right)}\right] \tag{3.22}$$

As $\cos(\sec^{-1}\theta) = 1/\theta$, thus

$$\cos\left[\sqrt{\frac{qn_ia^2}{V_m\epsilon_{si}}} \times \frac{x}{2}\right]^2 = \exp\left(-\frac{\psi_1(x,y)-\psi_0(y)}{V_m}\right) \tag{3.23}$$

Taking natural log of both the sides of Eq. (3.23) and using Eq. (3.3), one gets

$$\psi_1(x,y) = \psi_0(y) - \frac{2kT}{q}\ln\left[\cos\left(\sqrt{\frac{q^2n_i^2}{k_BTN_a\epsilon_{si}}\exp\left(\psi_0(y)-V_{ch}(y)\right)} \times \frac{x}{2}\right)^2\right] \tag{3.24}$$

Eq. (3.24) represents the potential caused by the inversion carries. To evaluate the potential contributed by the bulk carries, consider

$$\frac{\partial^2\psi_2(x,y)}{\partial x^2} = \frac{qN_a}{\epsilon_{si}} \tag{3.25}$$

Integrating Eq. (3.25) twice and using boundary conditions $\psi_2(x=0,y=0)=0$ and $\partial\psi_2(x,y)/\partial x|_{x=y=0}=0$, one gets

$$\psi_2(x,y) = \frac{qN_ax^2}{2\epsilon_{si}} \tag{3.26}$$

By combining Eqs. (3.4), (3.24) and (3.26), total surface potential of a 2D FET is given by

$$\psi(x,y) = \psi_0(y) - \frac{2kT}{q}\ln\left[\cos\left(\frac{x}{2}\sqrt{\frac{q^2n_i^2}{k_BTN_a\epsilon_{si}}\exp\left(\psi_0(y)-V_{ch}(y)\right)}\right)^2\right] + \frac{qN_ax^2}{2\epsilon_{si}} \tag{3.27}$$

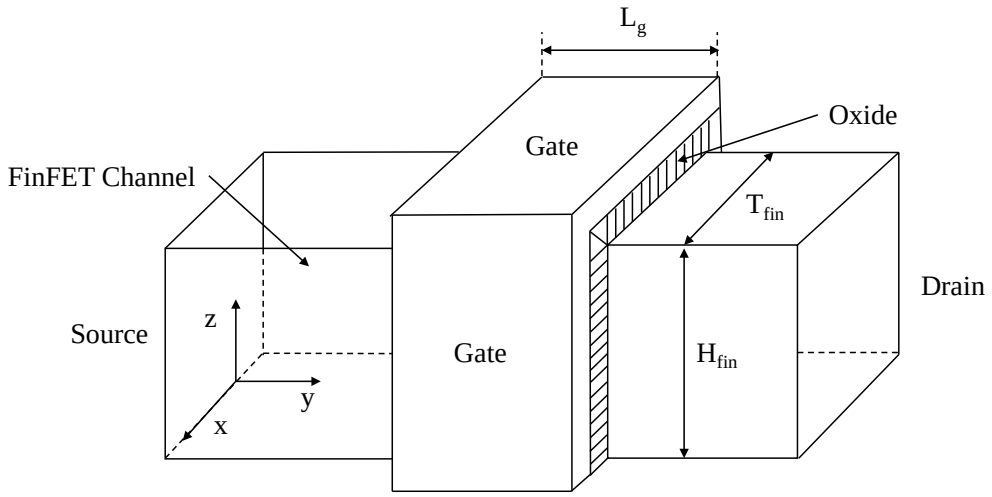

FIGURE 3.2: Electrical channel of a tri-gate Si FinFET.

3.2.2 3D Surface Potential Model

Consider the electrical channel of a FinFET shown in Fig. 3.2. In FinFET devices, H_{fin} plays an important role in determining the device characteristics. An acceptable design requires $H_{fin} \leq 3T_{fin}$ [105]. The surface potential evaluation of a FinFET device having $H_{fin} \geq 3T_{fin}$ differs from devices having $H_{fin} < 3T_{fin}$. For relatively high H_{fin} devices, z directed field could play an important role in determining the overall electrical characteristics of the device. A 3D surface potential of a FinFET device can be expressed as

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2} + \frac{\partial^2\psi(x,y,z)}{\partial y^2} + \frac{\partial^2\psi(x,y,z)}{\partial z^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi(x,y,z) + \phi_B - V_{ch}(y)}{V_m}\right) + \frac{qN_a}{\epsilon_{si}} \tag{3.28}$$

In short channel devices ($H_{fin} \geq 3T_{fin}$), the channel potential distribution can be expressed as

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi(x,y,z) + \phi_B - V_{ch}(y)}{V_m}\right) + \frac{qN_a}{\epsilon_{si}} \tag{3.29}$$

The solution of Eq. (3.29) is the same as given by Eq. (3.27). To evaluate y and z directed fields, one can proceed as

$$\frac{\partial^2\psi(x,y,z)}{\partial y^2} + \frac{\partial^2\psi(x,y,z)}{\partial z^2} = 0 \tag{3.30}$$

By separation of variables, lets assume the solution to Eq. (3.30) is $\psi(x,y,z) = Y(x,y)\ Z(x,z)$. Substituting the solution one gets

$$\frac{\partial^2 Y(x,y)Z(x,y)}{\partial y^2} = -\frac{\partial^2 Y(x,y)Z(x,z)}{\partial z^2} = -\alpha^2 \tag{3.31}$$

where, $\alpha^2 = \pi/(2L_g)$. We get a combination of two partial differential equations

$$\frac{\partial^2 Y(x,y)}{\partial y^2} + \alpha^2 Y(x,y) = 0 \tag{3.32}$$

$$\frac{\partial^2 Z(x,z)}{\partial z^2} - \alpha^2 Z(x,z) = 0 \tag{3.33}$$

Solution of Eqs. (3.32) and (3.33) can be expressed as

$$Y(x,y) = c_3\cos(\alpha y) + c_4\sin(\alpha y) \tag{3.34}$$

$$Z(x,z) = c_5\exp(-\alpha z) + c_6\exp(\alpha z) \tag{3.35}$$

The boundary conditions are $Y(x,0) = \phi_s$, $Y(x,L_g) = \phi_d$, $Z(x,0) = \psi(x,y)$ and $Z(0,H_{fin}) = \phi_B$. By using the boundary conditions and assuming $\acute{z} = (L_g/H_{fin})z$, Eq. (3.34) gives

$$Y(x,0) = c_3 = \phi_s \tag{3.36}$$

and

$$Y(x,L_g) = c_4 = \phi_d \tag{3.37}$$

By combining Eqs. (3.34), (3.36) and (3.37)

$$Y(x,y) = \phi_s\cos(\alpha y) + \phi_d\sin(\alpha y) \tag{3.38}$$

Now, employing the boundary conditions on Eq. (3.35), one gets

$$Z(x,0) = c_5 + c_6 = \psi(x,y) \tag{3.39}$$

and

$$Z(0,H_{fin}) = c_5\exp(-\pi/2) + c_6\exp(\pi/2) = \phi_B \tag{3.40}$$

Simultaneously solving Eqs. (3.39) and (3.40) gives

$$c_5 = \psi(x,y) - \frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)} \tag{3.41}$$

and

$$c_6 = \frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)} \tag{3.42}$$

Finally, combining Eqs. (3.35), (3.41) and (3.42) gives

$$\begin{aligned} Z(x,\acute{z}) = &\left[\psi(x,y) - \frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)}\right]\exp(-\alpha_1\acute{z}) \\ &+ \left[\frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)}\right]\exp(\alpha_1\acute{z}) \end{aligned} \tag{3.43}$$

where, $\alpha_1 = \pi/(2H_{fin})$ and total surface potential is given combining Eqs. (3.27), (3.38) and (3.43)

$$\begin{aligned} \psi(x,y,\acute{z}) =&\psi(x,y) + [\phi_s\cos(\alpha y) + \phi_d\sin(\alpha y)]\left[\frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)}\exp(\alpha_1\acute{z})\right. \\ &\left. + \left(\psi(x,y) - \frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)}\right)\exp(-\alpha_1\acute{z})\right] \end{aligned} \tag{3.44}$$

To add the effect of V_{gs} to the surface potential, Gausses law is applied to the channel shown in Fig. 3.2

$$V_{gs} = V_{fb} + \psi(T_{fin}/2, y, H_{fin}) + \frac{\epsilon_{si}}{C_{ox}}\xi_x(T_{fin}/2, y, H_{fin}) + \frac{\epsilon_{si}}{C_{ox}}\xi_{\acute{z}}(T_{fin}/2, y, H_{fin}) \tag{3.45}$$

In Eq. (3.45), the y directed field is not taken into consideration as the depletion of the channel varies mostly in x and z direction. At any given y, the y directed field is approximately zero as field produced due to V_{gs} is in the $x-z$ plane, which is perpendicular to the y plane. Both x and z directed fields are obtained by differentiating Eqs. (3.27) and (3.43) with respect to x and z, respectively

$$\xi_{\acute{z}}(T_{fin}/2, y, H_{fin}) = -\left[\psi(x,y) - \frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)}\right]\exp(-\pi/2)\alpha_1 + \left[\frac{\phi_B - \exp(-\pi/2)\psi(x,y)}{\exp(\pi/2) - \exp(-\pi/2)}\right]\exp(\pi/2)\alpha_1 \tag{3.46}$$

and

$$\xi_x(T_{fin}/2, y, H_{fin}) = \frac{qN_aT_{fin}}{2\epsilon_{si}} + \sqrt{\frac{V_m q n_i}{\epsilon_{si}}\left[\exp\left(\frac{\psi(T_{fin}/2, y, H_{fin}) + \phi_B - V_{ch}}{V_m}\right) - \exp\left(\frac{\psi_0(y) + \phi_B - V_{ch}}{V_m}\right)\right]} \tag{3.47}$$

At $x = x_{dep} = T_{fin}/2$, we define a new variable

$$\beta = \sqrt{\frac{q^2 n_i^2}{k_B T N_a \epsilon_{si}}\exp(\psi_0(y) - V_{ch}(y))} \times \frac{T_{fin}}{4} \tag{3.48}$$

By substituting β in Eq. (3.45), which is the only unknown variable; Eq. (3.45) can be solved iteratively or analytically. At any given V_{ds} and V_{gs}, the value of β can be obtained and from it, $\psi_0(y)$ can be extracted. Surface potential can then be found by using Eq. (3.44).

3.2.3 $I-V$ Model

The proposed $I-V$ model is obtained by solving the drift equation which is expressed as [106]

$$I_d(y) = 2\mu(V)WQ_{inv}\frac{dV_{ch}}{dy} \tag{3.49}$$

The mobility, $\mu(V)$ is bias dependent and can be written as [107]

$$\mu(V) = \frac{\mu_0}{1 + [\theta(V_{gs} - V_{th})]^{\gamma}} \tag{3.50}$$

Q_{inv} is dependent upon Q_{total} and Q_{bulk} charges and it can simply be expressed as

$$Q_{inv} = Q_{total} - Q_{bulk} \tag{3.51}$$

where, by using Eq. (3.26) one can write

$$Q_{bulk} = qN_a x \tag{3.52}$$

and,

$$Q_{total} = C_{ox}(V_{gs} - V_{fb} - \psi) \tag{3.53}$$

Comparing Eqs. (3.45) and (3.53) reveals

$$Q_{total} = \epsilon_{si}\xi_x + \epsilon_{si}\xi_{\acute{z}} \tag{3.54}$$

Q_{total} can be divided into two parts

$$Q_x = \epsilon_{si}\xi_x \qquad \text{and} \qquad Q_{\acute{z}} = \epsilon_{si}\xi_{\acute{z}} \tag{3.55}$$

Consider

$$Q_{\acute{z}} = \epsilon_{si}\xi_{\acute{z}} \tag{3.56}$$

Taking derivative of Eq. (3.56) w.r.t Q_{inv}

$$\frac{\partial Q_{\acute{z}}}{\partial Q_{inv}} = \epsilon_{si}\frac{\partial \xi_{\acute{z}}}{\partial Q_{inv}} \tag{3.57}$$

Since $Q_x = \epsilon_{si}\xi_x$, making substitution from Eqs. (3.47), (3.51) and (3.52) gives

$$Q_{bulk} + Q_{invx} = Q_{bulk} + \sqrt{V_m q n_i \epsilon_{si}\left[\exp\left(\frac{\psi + \phi_B - V_{ch}}{V_m}\right) - \exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_m}\right)\right]} \tag{3.58}$$

where $Q_{invx} = Q_x - Q_{bulk}$. For heavily doped devices, $Q_{bulk} \approx \epsilon_{si}\xi_x$ and as a result $\psi >> \psi_0$, therefore

$$Q_{invx} + Q_{bulk} \approx \sqrt{V_m q n_i \epsilon_{si}\left[\exp\left(\frac{\psi + \phi_B - V_{ch}}{V_m}\right)\right] + Q_{bulk}^2} \tag{3.59}$$

Taking square of both sides of Eq. (3.59), one gets

$$Q_{invx}^2(Q_{invx} + 2Q_{bulk}) = V_m q n_i \epsilon_{si} \times \exp\left(\frac{\psi + \phi_B - V_{ch}}{V_m}\right) Q_{invx} \tag{3.60}$$

Finally

$$Q_{invx} = \sqrt{V_m q n_i \epsilon_{si}} \times \exp\left(\frac{\psi + \phi_B - V_{ch}}{2V_m}\right)\sqrt{\frac{Q_{invx}}{Q_{invx} + 2Q_{bulk}}} \tag{3.61}$$

Now, taking derivative of Eq. (3.61) w.r.t Q_{inv}

$$\begin{aligned}\frac{\partial Q_{invx}}{\partial Q_{inv}} =& \frac{\sqrt{V_m q n_i \epsilon_{si}}}{2V_m} \times \exp\left(\frac{\psi + \phi_B - V_{ch}}{2V_m}\right)\sqrt{\frac{Q_{invx}}{Q_{invx} + 2Q_{bulk}}} \\ &\times \left[\frac{\partial \psi}{\partial Q_{inv}} - \frac{\partial V_{ch}}{\partial Q_{inv}}\right] + \sqrt{V_m q n_i \epsilon_{si}} \times \exp\left(\frac{\psi + \phi_B - V_{ch}}{2V_m}\right) \\ &\left(\frac{-Q_{bulk}}{(Q_{invx} + 2Q_{bulk})^2}\right)\left(\sqrt{\frac{Q_{invx}}{Q_{invx} + 2Q_{bulk}}}\right)^{-1}\frac{\partial Q_{invx}}{\partial Q_{inv}}\end{aligned} \tag{3.62}$$

Combining Eqs. (3.61) and (3.62) reveals

$$Q_{invx}\frac{\partial V_{ch}}{\partial Q_{inv}} = Q_{invx}\frac{\partial \psi}{\partial Q_{inv}} - 2V_m\frac{\partial Q_{invx}}{\partial Q_{inv}} - 2V_m\frac{Q_{bulk}}{Q_{invx} + 2Q_{bulk}}\frac{\partial Q_{invx}}{\partial Q_{inv}} \tag{3.63}$$

As $Q_{inv} = Q_{invx} + Q_{invz}$ and $\partial Q_{inv}/\partial Q_{inv} = \partial Q_{invx}/\partial Q_{inv} + \partial Q_{invz}/\partial Q_{inv}$, therefore

$$Q_{invx}\frac{\partial V_{ch}}{\partial Q_{inv}} = Q_{invx}\frac{\partial \psi}{\partial Q_{inv}} - 2V_m\left[1 - \frac{\partial Q_{invz}}{\partial Q_{inv}}\right] - 2V_m\frac{Q_{bulk}}{Q_{invx} + 2Q_{bulk}}\left[1 - \frac{\partial Q_{invz}}{\partial Q_{inv}}\right] \tag{3.64}$$

where, $Q_{invz} = Q_{\acute{z}} - Q_{bulk}$. As $Q_{invx} >> Q_{invz}$, therefore, Eq. (3.64) can be written as

$$Q_{inv}\frac{\partial V_{ch}}{\partial Q_{inv}} \approx Q_{inv}\frac{\partial \psi}{\partial Q_{inv}} - 2V_m\left[1 - \frac{\partial Q_{invz}}{\partial Q_{inv}}\right] - 2V_m\frac{Q_{bulk}}{Q_{inv} + 2Q_{bulk}}\left[1 - \frac{\partial Q_{invz}}{\partial Q_{inv}}\right] \tag{3.65}$$

Now, I_{ds} can be found by integrating Eq. (3.49) upon the entire gate i.e. 0 to L_g

$$I_{ds} = 2\mu(V)\frac{W}{L_g}\int_{Q_{invs}}^{Q_{invd}} Q_{inv}\frac{\partial V_{ch}}{\partial Q_{inv}}\partial Q_{inv} \tag{3.66}$$

where Q_{invd} and Q_{invs} are inversion charges at drain and source terminals, respectively. By using Eqs. (3.65) and (3.66), the final expression of I_{ds} is obtained

$$I_{ds} = 2\mu(V)\frac{W}{L_g}(\acute{\psi}_d - \acute{\psi}_s) \tag{3.67}$$

where, the function $\acute{\psi}_s$ and $\acute{\psi}_d$ are represented, respectively, by

$$\begin{aligned}\acute{\psi}_s \approx & -\frac{Q_{invs}^2}{2C_{ox}} - 2V_m Q_{invs} - 2V_m Q_{bulk}\ln(Q_{invs} + 2Q_{bulk}) + 2V_m Q_{\acute{z}s} \\ & + 2V_m\frac{Q_{bulk}}{Q_{invs} + 2Q_{bulk}}Q_{\acute{z}s}\end{aligned} \tag{3.68}$$

and

$$\begin{aligned}\acute{\psi}_d \approx & -\frac{Q_{invd}^2}{2C_{ox}} - 2V_m Q_{invd} - 2V_m Q_{bulk}\ln(Q_{invd} + 2Q_{bulk}) + 2V_m Q_{\acute{z}d} \\ & + 2V_m\frac{Q_{bulk}}{Q_{invd} + 2Q_{bulk}}Q_{\acute{z}d}\end{aligned} \tag{3.69}$$

While writing the above expressions, the integration term involving $Q_{\acute{z}}Q_{bulk}/(Q_{inv} + 2Q_{bulk})^2 \approx 0$ as $Q_{bulk} >> Q_{\acute{z}} >> Q_{inv}$. In Eqs. (3.68) and (3.69) $Q_{\acute{z}s}$ and $Q_{\acute{z}d}$ are the total source and drain charges due to field $\xi_{\acute{z}}$. Eq. (3.67) can be used to plot the $I - V$ characteristics of a FinFET as a function of both V_{ds} and V_{gs}.

TABLE 3.1: Physical parameters of different devices used in this study.

Parameters	T_1 [108]	T_2 [109]	T_3 [110]
L_g (nm)	45	4000	50
T_{fin} (nm)	30	22	10
H_{fin} (nm)	100	230	70
H_{fin}/T_{fin}	3.34	10.5	7
W (nm)	30	600	10
T_{ox} (nm)	2.0	7.5	2.5
N_a (x 10^{24} m^{-3})	1.0	0.001	0.001
V_{th} (V)	0.68	1.4	0.2

3.3 Results and Discussion

To validate the derived expression of the $I-V$ curve, Si based FinFETs were chosen and their details are given in Table 3.1. As seen from the table, devices of various physical dimensions were selected in order to fully study the model's validity. In FinFETs, the long and short channel devices are not merely defined by the L_g of the device, rather the distinction is made on the basis of the overall area present for the channel current and the ratio of H_{fin} to T_{fin}. Devices T_2 and T_3, are described as short channel devices, while device T_1 is a relatively long channel device.

TABLE 3.2: Physical constants used in this study.

Parameters	**Value**
n_i (x 10^{21} m^{-3})	1
k_B ($J.K^{-1}$)	1.38
T (K)	300
q (x 10^{-19} C)	1.6
μ_0 ($m^2V^{-1}s^{-1}$)	0.14
ϵ (x 10^{-12} Fm^{-1})	8.85
ϵ_{si}	11.68ϵ
ϵ_{ox}	3.9ϵ

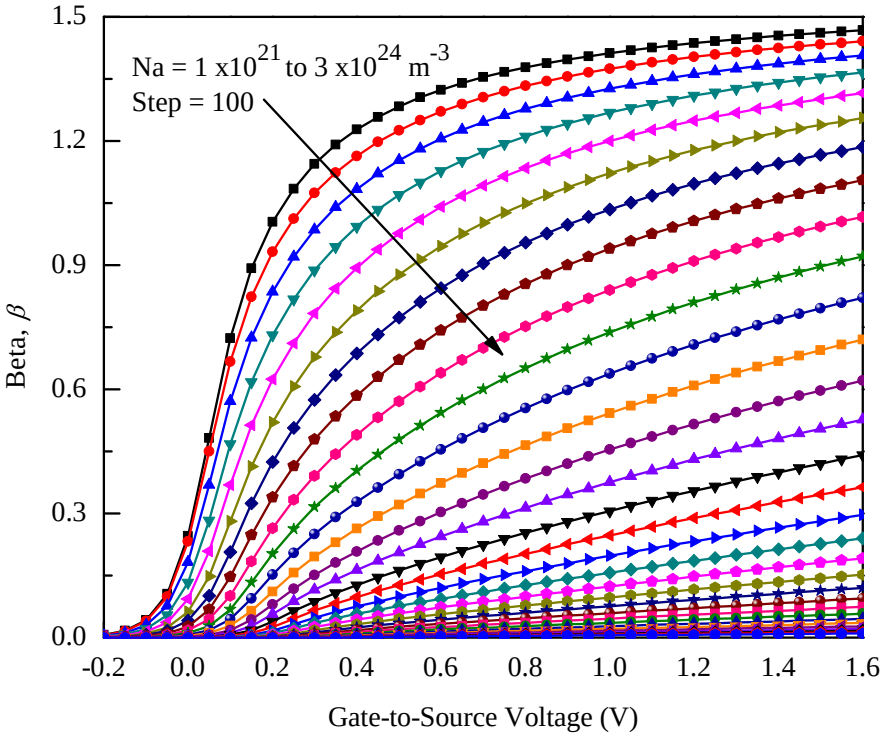

FIGURE 3.3: Variation in the variable β with N_a and applied V_{gs} at $V_{ds} = 0$ V.

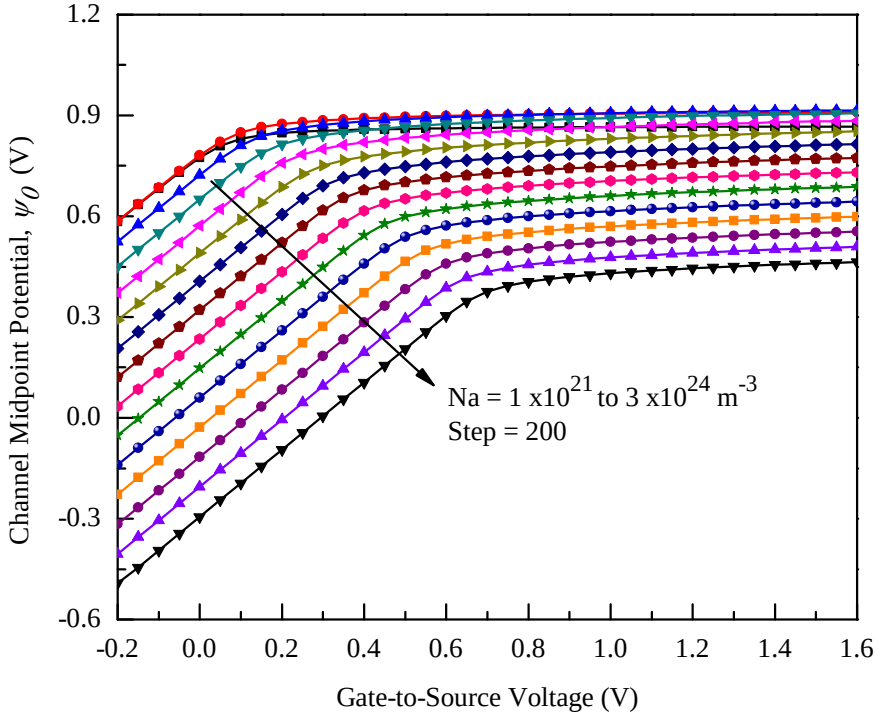

FIGURE 3.4: Variation in midpoint channel potential, $\psi_0(y)$ with V_{gs} and N_a at $V_{ds} = 0$ V.

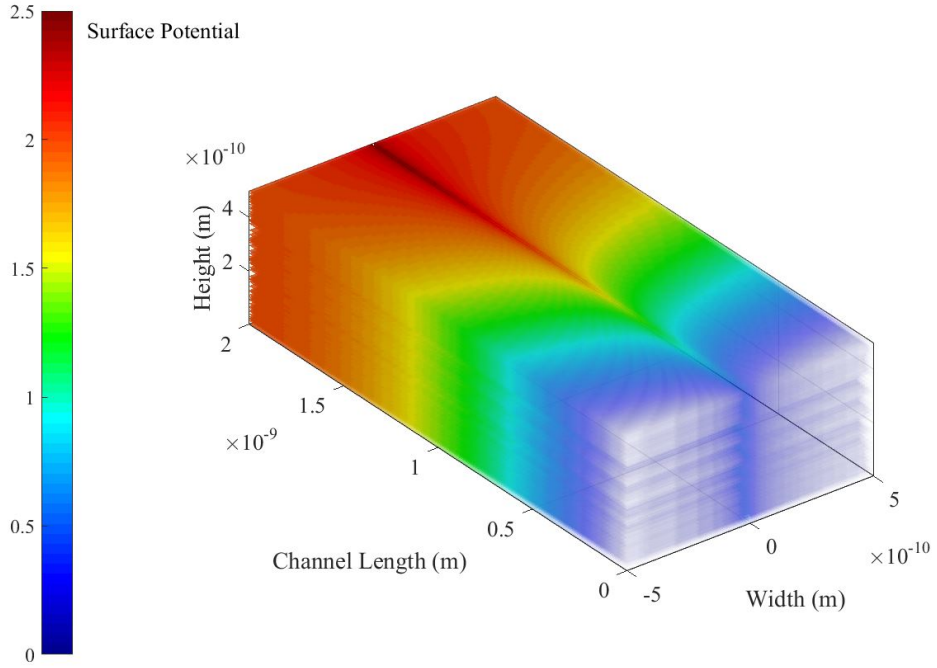

FIGURE 3.5: Potential distribution inside the channel of a Si FinFET at $V_{gs} = 0$ V and $V_{ds} = 2$ V.

In order to simulate the $I - V$ characteristics first, Eq. (3.45) must be solved to get the value of β. Figure 3.3 shows the variation of β when V_{gs} is varied, keeping V_{ds} constant. At lower N_a, β increases with the increase in V_{gs} and then saturates to a constant value. On the other hand, increasing N_a, causes β to decrease and also, the linear region of β increases. The same variation in $\psi_0(y)$ can be observed from the plot of Fig. 3.4, which is calculated using the value of β at $x = T_{fin}/2$.

Figure 3.5 shows the variation of surface potential inside the FinFET channel as predicted by Eq. (3.44). The figure clearly represents the transition of drain potential to source potential when $V_{ds} = 2$ V is applied across the drain-source terminals. At $x = T_{fin}/2$, $y = L_g/2$ and $z = H_{fin}$, the variation in channel potential for both the proposed model and BSIM-CMG model [97] is shown by Fig. 3.6. Studying the figure, it can be observed that at lower N_a, both, the techniques result in similar values of ψ, but when N_a is increased, a discrepancy between BSIM-CMG and the proposed technique is evident. This variation can be explained by the proposed Eq. (3.44), where the effect of x, y, z; all the three dimensions are incorporated in determining ψ.

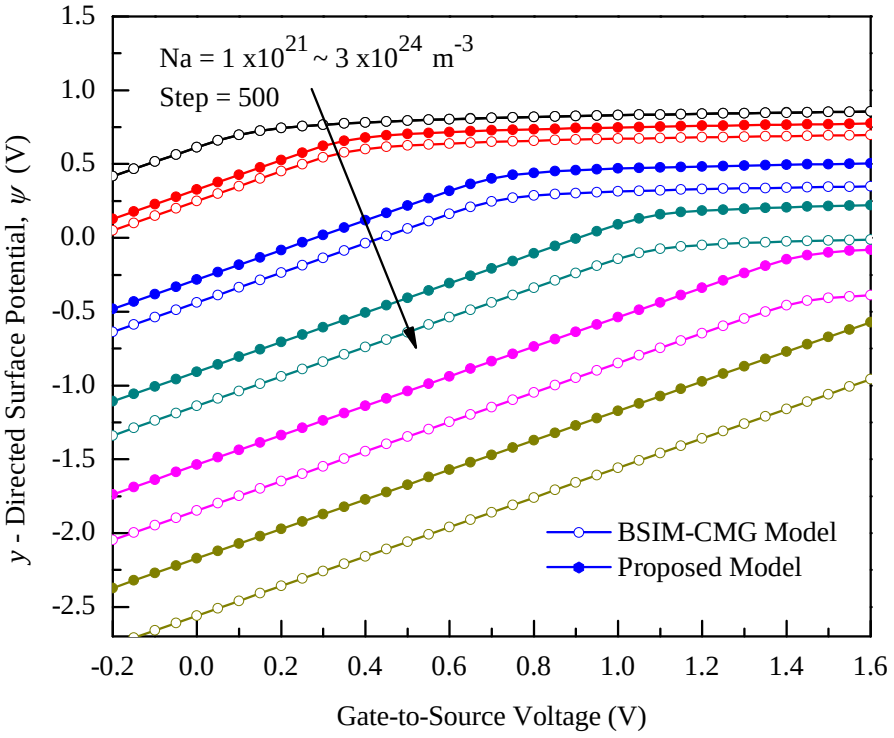

FIGURE 3.6: Change in surface potential with respect to N_a and applied V_{gs} at $V_{ds} = 0$ V.

Eq. (3.67) is used to plot the $I - V$ response of the devices mentioned in Table. 3.1. Constant parameters associated with Eq. (3.67) are mentioned in Table. 3.2. These parameters are treated as constants throughout the modeling process and are same for each of the chosen devices.

Figure 3.7 (a) shows the comparison of modeled $I-V$ characteristics with the data of device T_1. Both the proposed and BSIM-CMG models show good accuracy in predicting the $I - V$ response of the device at relatively small V_{gs} values however, at $V_{gs} = 2$ V for the BSIM-CMG model, there is a noticeable discrepancy in the saturation region of operation. The accuracy of the proposed technique can be associated with the estimation of surface potential involving the entire geometry of the device. As V_{gs} of the device increases, the z directed field cannot be ignored as it starts to play a crucial role in the channel behavior.

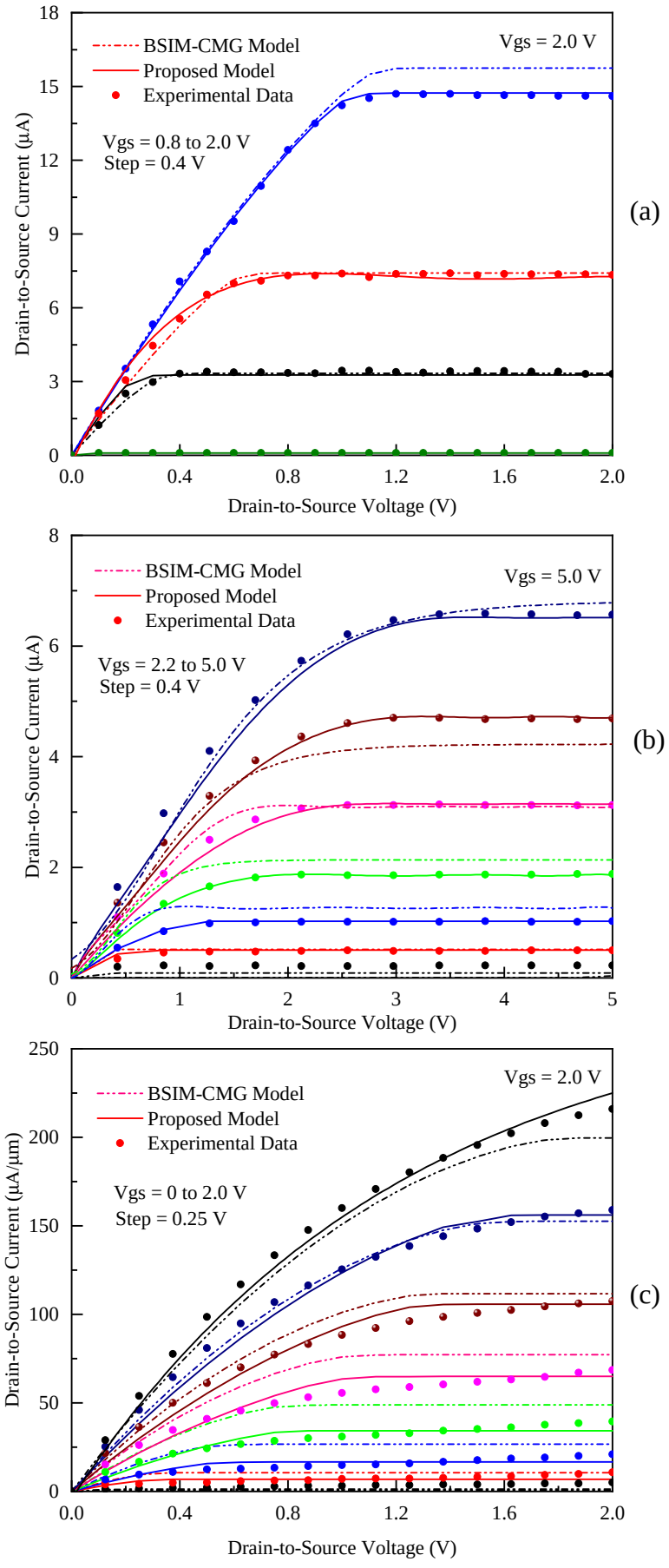

FIGURE 3.7: Comparison between modeled and experimental $I-V$ characteristics of a Si FinFET having T_{fin}: a) 30 nm, b) 22nm and c) 10nm.

TABLE 3.3: Comparison of root mean square error (RMSE x 10^{-10}) of analytical models used to predict $I-V$ characteristics of device T_1.

Model	V_{gs} **(V)**				**Avg.**
	0.05	**1.2**	**1.5**	**2.0**	
Proposed	1.01	1.56	2.11	1.55	1.65
BSIM-CMG	1.03	1.57	2.10	1.67	1.76

TABLE 3.4: Comparison of root mean square error (RMSE x 10^{-10}) of analytical models used to predict $I-V$ characteristics of device T_2.

Model	V_{gs} **(V)**							**Avg.**
	2.6	**3.0**	**3.4**	**3.8**	**4.2**	**4.6**	**5.0**	
Proposed	2.02	0.49	0.64	0.95	1.59	2.28	2.80	16.6
BSIM-CMG	3.40	9.30	4.30	4.60	1.50	6.60	3.32	37.5

TABLE 3.5: Comparison of root mean square errors (RMSE x 10^{-10}) of analytical models used to predict $I-V$ characteristics of device T_3 .

Model	V_{gs} **(V)**								**Avg.**
	0.25	**0.50**	**0.75**	**1.00**	**1.25**	**1.50**	**1.75**	**2.00**	
Proposed	0.20	0.13	0.18	0.22	0.31	0.33	0.35	0.41	4.20
BSIM-CMG	0.18	0.23	0.71	1.00	1.03	0.67	0.27	0.71	8.24

Table 3.3 shows the comparison of both the models in terms of Root Mean Square Error (RMSE). RMSE is calculated by employing the following equation

$$\text{RMSE} = \sqrt{\sum_{Q=N_1}^{N_2} \left\{ \sum_{P=M_1}^{M_2} \left(I_{DS(exp)}^{P,Q} - I_{DS(mod)}^{P,Q} \right)^2 \Bigg/ \sum_{P=M_1}^{M_2} I_{DS(exp)}^{P,Q} \right\}} \tag{3.70}$$

where, $I_{DS(exp)}$ and $I_{DS(mod)}$ are the experimental and modeled values of I_{ds}, respectively, P and Q represent V_{ds} and V_{gs} having minimum value M_1 and N_1; maximum value M_2 and N_2, respectively. As observed from the data of the table, there is a slight improvement in $I-V$ prediction by using the proposed model. At lower V_{gs}, both the models behave the same while at higher V_{gs}, the proposed technique show less error as is evident from Fig. 3.7 (a).

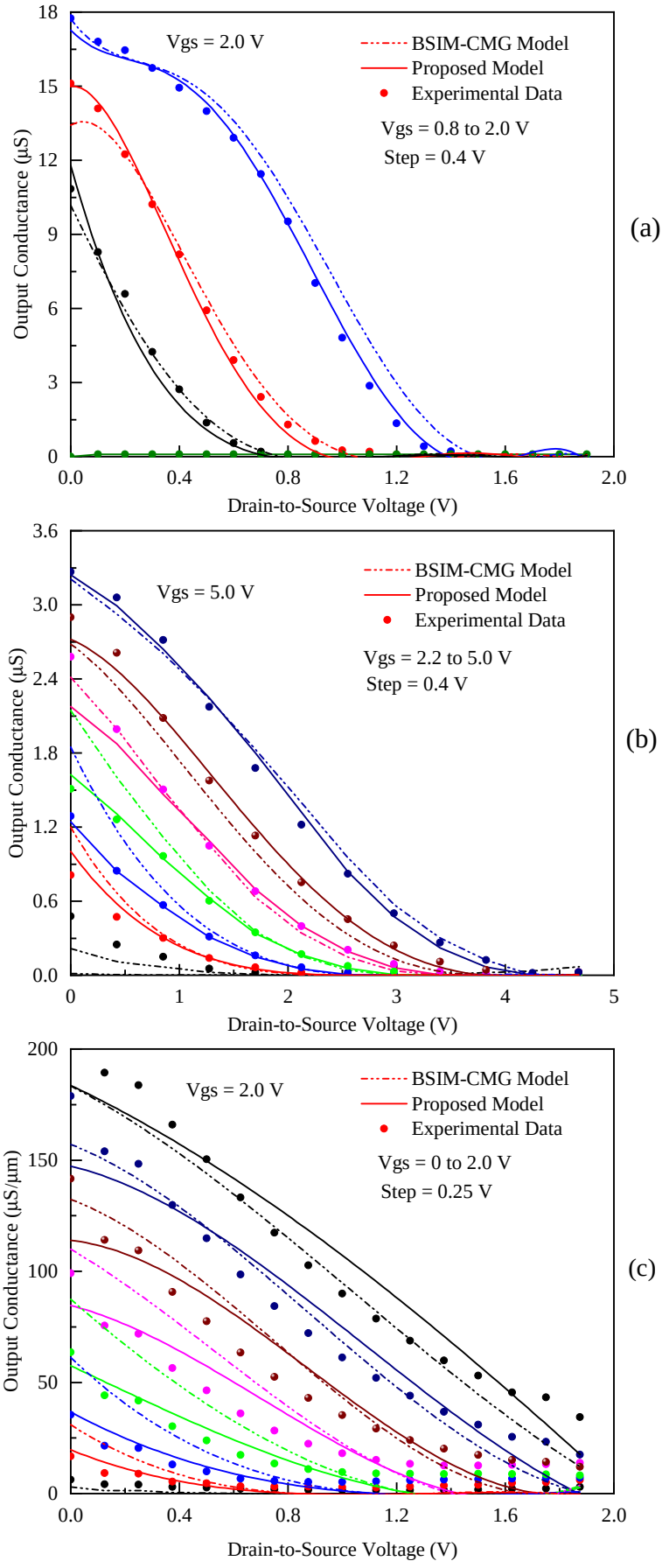

FIGURE 3.8: Comparison between modeled and experimental output conductance of Si FinFETs having T_{fin}: a) 30 nm, b) 22 nm and c) 10 nm.

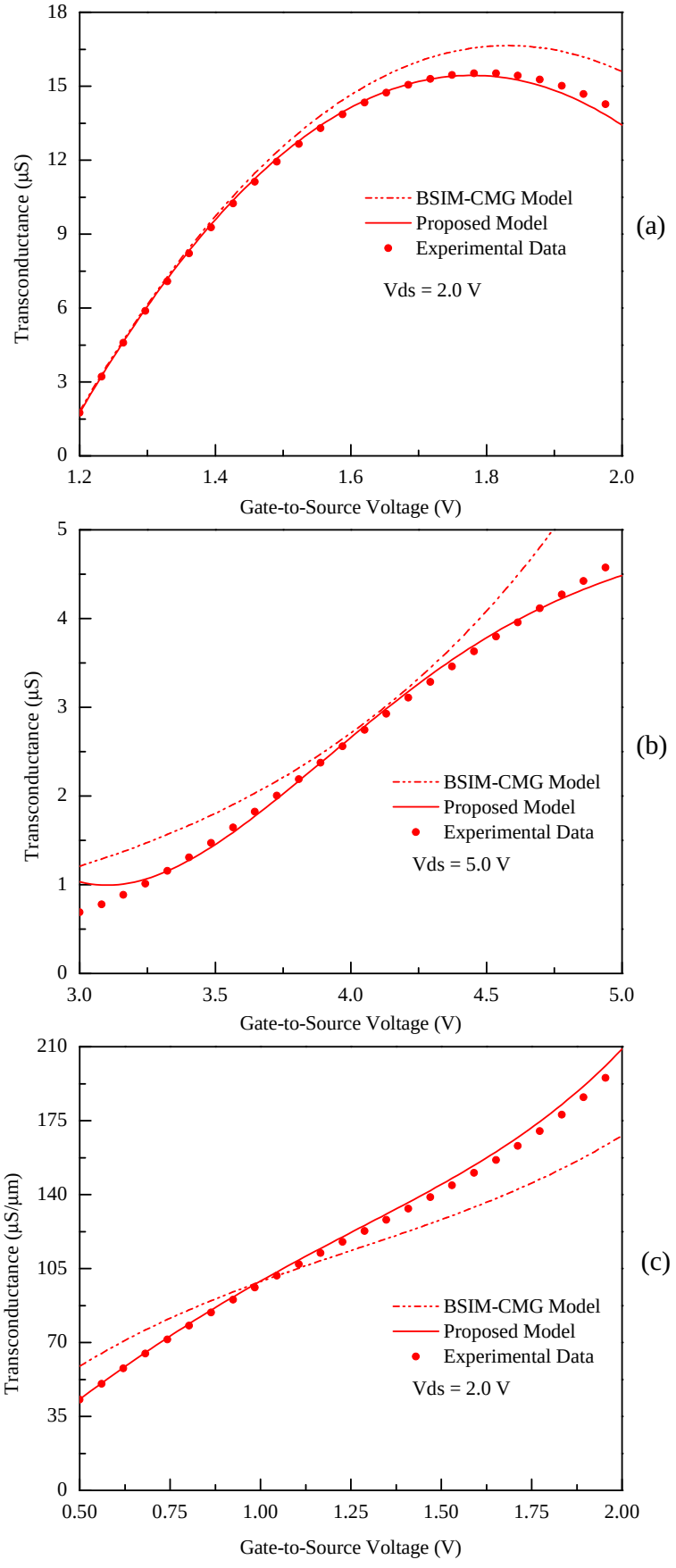

FIGURE 3.9: Comparison between modeled and experimental transconductance of Si FinFETs having T_{fin}: a) 30 nm, b) 22 nm and c) 10 nm.

Figure 3.7 (b) plots the results of both the models for device T_2. It can be seen that there is significant error between BSIM-CMG and the experimental data, while the proposed technique predicts the characteristics with better accuracy. This is also validated by Table 3.4, as the average RMSE for the proposed technique is significantly lower than the BSIM-CMG model. Although the over all channel area of device T_2 is large, T_{fin} plays an important role in the model. At lower values of T_{fin}, the x directed width of the channel shrinks and most of the current starts flowing through the $y-z$ plane. As BSIM-CMG model ignores the z direction, an increase in RMSE is therefore, observed when $H_{fin} \gg T_{fin}$.

Figure 3.7 (c) shows the data of device T_3 and its comparison with the models under discussion. As T_3 is a short channel device, thus $z-$directed field plays an important role in its characteristics. It is evident from the figure and Table 3.5 that the proposed model once again gives a relatively better performance in predicting the output characteristics of a short channel FinFET. Almost at every V_{gs} value, the proposed model outperforms the BSIM-CMG technique. By examining the data of the table, it is observed that the proposed technique offers $\sim 45\%$ reduction in RMSE value. Thus, the proposed model can be a preferred choice to predict the $I-V$ characteristics of both long and short channel Si FinFETs.

Figure 3.8 compares the output conductance of all the devices under discussion. It can be observed that under every condition, the proposed model exhibits better performance than its BSIM-CMG counter part. Similarly, Fig. 3.9 shows the transconductance characteristics predicted by both the models. The same result is evident from the graphs, that the proposed technique offers better results compared to the BSIM-CMG technique. Thus, examining all the figures (Figs. 3.7-3.9), it can be concluded that the proposed technique is relatively better in predicting the $I-V$ characteristics than BSIM-CMG model.

3.4 Summary

In this chapter, a 3D surface potential model is presented to evaluate $I-V$ characteristics of Si FinFETs. The model evaluates the potential distribution of a FinFET by solving a 3D Poisson equation, which complies to the geometry of the device. Knowing the device potential and charge concentration inside the channel, an $I-V$ expression is developed, which can predict the characteristics both for undoped and doped FinFETs. In order to establish the general applicability of the proposed model, it has been checked on the experimental data of FinFETs of varying dimensions. It has been observed that the proposed model offers $6-45\%$ improvement in predicting the $I-V$ characteristics of FinFETs with respect to the best model reported in literature. Thus, the proposed model can be employed in software tools meant to predict $I-V$ characteristics of Si FinFETs.

Chapter 4

Independent Gate FinFETs Model

4.1 Introduction

FinFET is a promising new candidate for future technology due to its ability to control the channel of the device with relative ease compared to conventional FETs [111–113]. FinFETs are divided into two major categories depending on the gate of the device. Single gate FinFETs are controlled by one gate electrode while, multiple gate FinFETs (MG-FinFETs) can be controlled by more than one gate acting on the device independently [114, 115]. MG-FinFETs offer more flexibility in circuit design compared to single gate FinFETs.

MG-FinFETs are employed to control effectively V_{th} [116], conversion gain [117] and power management [118] in large nano circuities. Due to the 3D structure of FinFETs, the height and effective width ($W_{\text{eff}} = 2H_{fin} + T_{fin}$) of the device is always correlated and increasing one will also effect the other in a quantized fashion as all the fins must be of the same height due to the fabrication process limitations [105, 119]. Using MG-FinFETs, width quantization effect on large circuits, such as SRAMs can be reduced [120, 121]. Also, in independent gate SRAMs, the dual

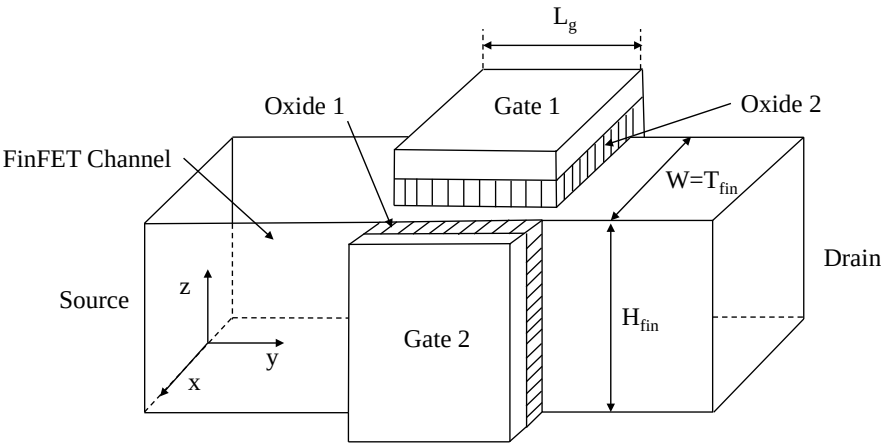

FIGURE 4.1: An independent gate FinFET device.

gate system acts as a built-in feedback network and reduces read/write margins [122, 123].

To fully comprehend the device behavior, models specific to independent gate FinFETs are needed. Researchers have developed many models for the characteristics of MG-FinFETs [124–126], but to the best of our knowledge, none of the models take into account the effect of channel height on the device characteristics.

In this chapter, a DC model is presented for MG-FinFET devices. Poisson's equation is solved to estimate the potential distribution inside the channel by taking into consideration, the effect of channel height, and by using drift equation and channel potential, current flowing through the device is calculated. The following sections describe the model formation and the results obtained from them. A discussion is also presented on the basis of the results obtained and finally, conclusions associated with the study are derived.

4.2 Model Development

4.2.1 Surface Potential Model

Figure 4.1 shows an independent MG-FinFET device. From the figure, it can be observed that two individual gate potentials are acting on the channel of the

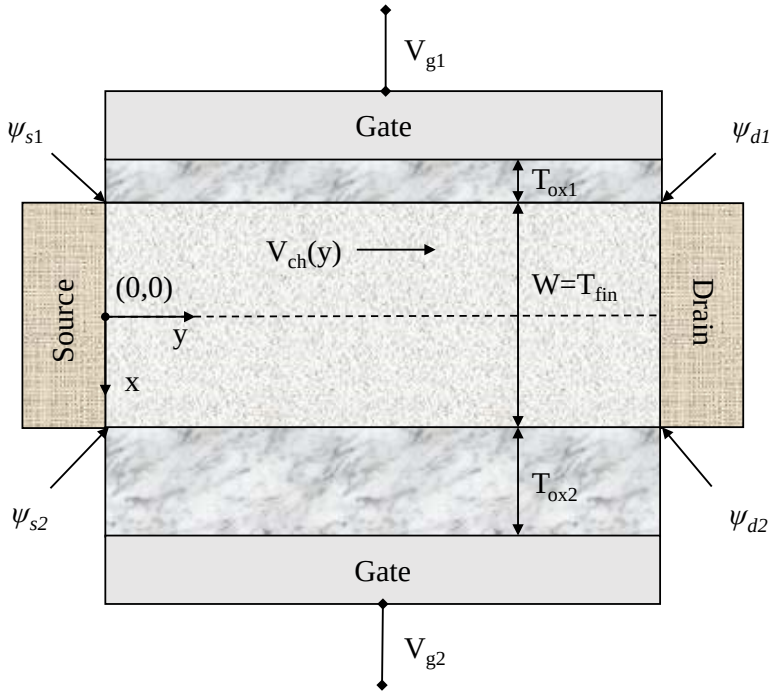

FIGURE 4.2: Crossectional view of an independent gate FinFET device.

FinFET. This can easily be visualized from Fig. 4.2, where the $x-y$ crossection of Fig. 4.1 is illustrated.

Potential distribution inside the channel of a MG-FinFET can be expressed using Poisson's equation with appropriate boundary conditions. The Poisson's equation representing the potential distribution inside the channel takes into account, the dependence of both inversion and bulk charges on surface potential and can be expressed as

$$\frac{\partial^2\psi_x}{\partial x^2}+\frac{\partial^2\psi_z}{\partial z^2}=\frac{qn_i}{\epsilon_{si}}\exp\left(\frac{\psi+\phi_B-V_{ch}}{V_m}\right)+\frac{qN_a}{\epsilon_{si}} \tag{4.1}$$

where

$$\phi_B=V_m\ \ln\left(\frac{N_a}{n_i}\right) \tag{4.2}$$

and

$$V_m=\frac{k_BT}{q} \tag{4.3}$$

$V_{ch}(y)$, shown in Fig. 4.2, determines the drain to source potential at any given value of y, and it can vary from $V_{ch}(0)=0$ to $V_{ch}(L_g)=V_{ds}$. As channel depletion

varies mostly in the x-direction therefore,

$$\frac{\partial^2 \psi_z}{\partial z^2} \approx 0 \tag{4.4}$$

Equation (4.4) can be integrated to get

$$\xi_z = \frac{\partial \psi_z}{\partial z} = \frac{V_{gs1}}{H_{fin}} \qquad \text{and} \qquad \psi_z = \frac{V_{gs1}}{H_{fin}} z \tag{4.5}$$

Eq. (4.5) is attained by using boundary conditions

$$\psi_z(0,0,0) = 0 \qquad \text{and} \qquad \psi_z(0,0,H_{fin}) = V_{gs1} \tag{4.6}$$

Considering Eq. (4.1), the x-directed potential can be written as

$$\frac{\partial^2 \psi_x}{\partial x^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi + \phi_B - V_{ch}}{V_m}\right) + \frac{qN_a}{\epsilon_{si}} \tag{4.7}$$

subjected to boundary conditions

$$\left.\frac{\partial \psi_x(x,y,z)}{\partial x}\right|_{x=z=0} = 0 \quad \text{and} \quad \psi_x(x=0,y,z=0) = \psi_0(y) \tag{4.8}$$

Integrating Eq. (4.7) and by applying boundary conditions given by Eq. (4.8), one can get

$$\xi_x = \frac{\partial \psi_x}{\partial x} = \left[\frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi + \phi_B - V_{ch}}{V_m}\right) - \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_m}\right)\right]^{1/2} \tag{4.9}$$

The potential is applied on each gate independently thus, it must be treated separately. Assuming that ψ_1 is the potential due to V_{gs1} and ψ_2 is the potential due to V_{gs2}. By keeping that in mind, Eq. (4.9) can be written for both gates as

$$\xi_{x1} = \frac{\partial \psi_1}{\partial x} = \left[\frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right) - \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_m}\right)\right]^{1/2} \tag{4.10}$$

and

$$\xi_{x2} = \frac{\partial \psi_2}{\partial x} = \left[\frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m} \right) - \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_m} \right) \right]^{1/2} \tag{4.11}$$

To eliminate the dependence of ξ_{x1} and ξ_{x2} on $\psi_0(y)$, both Eqs. (4.10) and (4.11) are squared, and subtracted from each other resulting in

$$\xi_{x1}^2 - \xi_{x2}^2 = \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m} \right) - \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m} \right) \tag{4.12}$$

By applying Gauss's law on both the gates, the x-directed fields can be expressed as

$$\xi_{x1} = \frac{C_{ox1}}{\epsilon_{si}} [V_{gs1} - V_{fb1} - \psi_1] - \xi_z \tag{4.13}$$

and

$$\xi_{x2} = \frac{C_{ox2}}{\epsilon_{si}} [V_{gs2} - V_{fb2} - \psi_2] \tag{4.14}$$

where

$$C_{ox1} = \frac{\epsilon_{ox1}}{T_{ox1}} \qquad \text{and} \qquad C_{ox2} = \frac{\epsilon_{ox2}}{T_{ox2}} \tag{4.15}$$

To find ψ_1 and ψ_2, it is assumed that the potential ψ_2 exits due to the weak inversion of carriers and by using the capacitor distribution on both the gates, ψ_2 can be evaluated as

$$\psi_2 = \alpha \psi_1 + \beta (V_{gs2} - V_{fb2}) \tag{4.16}$$

where

$$\alpha = \frac{C_{si}}{C_{si} + C_{ox2}}$$

$$\beta = \frac{C_{ox2}}{C_{si} + C_{ox2}} \tag{4.17}$$

$$C_{si} = \frac{\epsilon_{si}}{T_{fin}}$$

In order to find ψ_1, Eqs. (4.12), (4.13), (4.14) and (4.16) are combined to get

$$\begin{aligned}
&\left(\frac{C_{ox1}}{\epsilon_{si}}[V_{gs1} - V_{fb1} - \psi_1] - \xi_z\right)^2 \\
&- \left(\frac{C_{ox2}}{\epsilon_{si}}[V_{gs2} - V_{fb2} - (\alpha\psi_1 + \beta(V_{gs2} - V_{fb2}))]\right)^2 \\
&- \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right) \\
&+ \frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\alpha\psi_1 + \beta\psi_1[V_{gs2} - V_{fb2}] + \phi_B - V_{ch}}{V_m}\right) = 0
\end{aligned} \tag{4.18}$$

Equation (4.18) can be solved iteratively to get the value of ψ_1 and by putting ψ_1 is Eq. (4.16), ψ_2 is obtained.

4.2.2 $I - V$ Model

The proposed $I - V$ model utilizes drift equation and is given by

$$I_{ds} = 2\mu(V)\frac{W}{L_g}\int_0^{L_g} Q_{inv}\frac{\partial V_{ch}}{\partial y}\partial y \tag{4.19}$$

The inversion charge can be expressed as

$$Q_{inv} = \epsilon_{si}(\xi_{x1} - \xi_{x2} + \xi_z) - Q_{bulk} \tag{4.20}$$

where,

$$Q_{bulk} = qN_a x \tag{4.21}$$

From Eq. (4.12)

$$\begin{aligned}
\epsilon_{si}\xi_{x1} = \Bigg[V_m q n_i \epsilon_{si}\Bigg[&\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right) \\
&- \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m}\right)\Bigg] + (\epsilon_{si}\xi_{x2})^2\Bigg]^{1/2}
\end{aligned} \tag{4.22}$$

Combining Eqs. (4.20) and (4.22), one can get

$$Q_{inv} = \left[V_m q n_i \epsilon_{si} \left[\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right) - \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m}\right)\right] + (\epsilon_{si}\xi_{x2})^2\right]^{1/2}$$

$$- \epsilon_{si}\xi_{x2} + \epsilon_{si}\xi_z - Q_{bulk} \tag{4.23}$$

Differentiating Eq. (4.23) w.r.t y

$$\frac{\partial Q_{inv}}{\partial y} = \frac{1}{2V_m K_1}\left[\gamma \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m}\right) - \gamma \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right)\right]\frac{\partial V_{ch}}{\partial y}$$

$$+ \frac{1}{2V_m K_1}\left[\gamma \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right)\frac{\partial \psi_1}{\partial y} - \gamma \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m}\right)\frac{\partial \psi_2}{\partial y}\right] \tag{4.24}$$

where,

$$K_1 = Q_{inv} + \epsilon_{si}\xi_{x2} - \epsilon_{si}\xi_z + Q_{bulk} \quad \text{and} \quad \gamma = V_m q n_i \epsilon_{si} \tag{4.25}$$

and $\partial\xi_{x2}/\partial y \approx 0$. For doped body, $\psi_1, \psi_2 >> \psi_0$ therefore, Eqs. (4.10) and (4.11) can be rewritten as

$$\xi_{x1} \approx \sqrt{\frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_1(x,y,z) + \phi_B - V_{ch}(y)}{V_m}\right)} \tag{4.26}$$

and

$$\xi_{x2} \approx \sqrt{\frac{V_m q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_2(x,y,z) + \phi_B - V_{ch}(y)}{V_m}\right)} \tag{4.27}$$

Now, considering Eq. (4.23)

$$V_m q n_i \epsilon_{si}\left[\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_m}\right) - \exp\left(\frac{\psi_2 + \phi_B - V_{ch}}{V_m}\right)\right] = K_2 \tag{4.28}$$

where,

$$K_2 = K_1^2 - (\epsilon_{si}\xi_{x2})^2 \tag{4.29}$$

By using Eqs. (4.24), (4.26), (4.27) and (4.28)

$$Q_{inv}\frac{\partial V_{ch}}{\partial y} = \left(2V_m \frac{K_1}{K_2}\frac{\partial Q_{inv}}{\partial y} - \frac{K_3}{K_2}\frac{\partial \psi_1}{\partial y} + \frac{K_4}{K_2}\frac{\partial \psi_2}{\partial y}\right) Q_{inv} \tag{4.30}$$

where

$$K_3 = (\epsilon_{si}\xi_{x1})^2 \qquad \text{and} \qquad K_4 = (\epsilon_{si}\xi_{x2})^2 \tag{4.31}$$

For simplicity, $K_1/K_2 = \sigma_1$, $K_3/K_2 = \sigma_2$ and $K_4/K_2 = \sigma_3$. Now, by combining Eqs. (4.19) and (4.30), I_{ds} can be expressed as

$$I_{ds} = 2\mu(V)\frac{W}{L_g}\int_0^{L_g}\left(2V_m\sigma_1\frac{\partial Q_{inv}}{\partial y} - \sigma_2\frac{\partial \psi_1}{\partial y} + \sigma_3\frac{\partial \psi_2}{\partial y}\right)Q_{inv}\partial y \tag{4.32}$$

To simplify the expression (Eq. 4.32), it is approximated that the terms Q_{inv}, ξ_{x2} and ξ_z have their average values with respect to source and drain terminals, so

$$I_{ds} = 2\mu(V)\frac{W}{L_g}\Big[2V_m\sigma_1(Q_{invd} - Q_{invs}) - \sigma_2(\psi_{d1} - \psi_{s1}) + \sigma_3(\psi_{d2} - \psi_{s2})\Big]\frac{Q_{invd} + Q_{invs}}{2} \tag{4.33}$$

Equation (4.33) gives the final expression of current where, Q_{invs} and Q_{invd} are the charges accumulated at the source and drain terminals of the FinFET device, respectively. ψ_{d1} and ψ_{s1} are the drain and source potentials due to V_{gs1}, and ψ_{d2} and ψ_{s2} are the drain and source potentials due to V_{gs2}.

4.3 Results and Discussion

To verify the validity of the proposed model, independent gate FinFET devices of various dimensions were selected and their details are given by Tables 4.1 and 4.2. Equation (4.33) was used to plot the $I - V$ characteristics of the FinFETs.

Figure 4.3 shows the result of the modeled expression against simulated data for the device having $L_g = 100$ nm at $V_{gs2} = 0$ V. Form the figure, it is evident that the proposed model can simulate the characteristics of independent gate FinFETs with good accuracy. Figure 4.4 represents the $I - V$ characteristics of the device having L_g= 10.8 nm at $V_{gs2} = 0.7$ V. A good agreement is observed between the

TABLE 4.1: Physical parameters of independent gate FinFET devices used in this study.

Parameters	T_1 [124]	T_2 [127]
L_g (nm)	100	10.8
T_{fin} (nm)	15	4.5
H_{fin} (nm)	30	12.5
H_{fin}/T_{fin}	2.0	2.8
W (nm)	15	4.5
T_{ox1} (nm)	2.0	0.61
T_{ox2} (nm)	2.0	0.61
N_a (x 10^{24} m^{-3})	—	100
V_{th} (V)	0.5	0.3

TABLE 4.2: Physical constants for independent gate FinFETs used in this study.

Parameters	**Value**
n_i (x 10^{21} m^{-3})	1
k_B ($J.K^{-1}$)	1.38
T (K)	300
q (x 10^{-19} C)	1.6
μ ($m^2V^{-1}s^{-1}$)	0.11
ϵ (x 10^{-12} Fm^{-1})	8.85
ϵ_{si}	11.68ϵ
ϵ_{ox1}	3.9ϵ
ϵ_{ox2}	3.9ϵ

modeled and simulated plots. From the figures, it is also evident that the proposed model can accurately predict the $I-V$ characteristics when the applied bias and oxide thickness is varying. This solidifies the position of the proposed model, as it can anticipate the effect of changing V_{gs2} on the device characteristics.

Figures 4.5 and 4.6 show the output characteristics of devices T_1 and T_2, respectively. By studying the figure, it can be seen that the proposed technique has the ability to accurately find the output characteristics of the devices, both in linear and saturation regions of operation, irrespective of the device dimensions and applied bias.

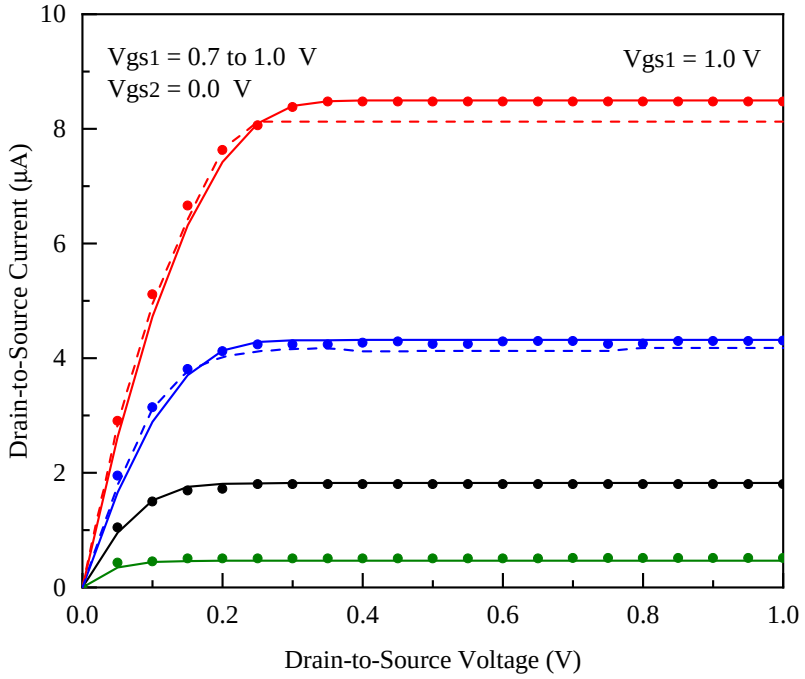

FIGURE 4.3: Comparison between modeled (Solid line: proposed model with the effect of height, Broken line: model without the effect of height [124]) and simulated (Dots) $I-V$ characteristics of an independent gate FinFET with L_g= 100 nm.

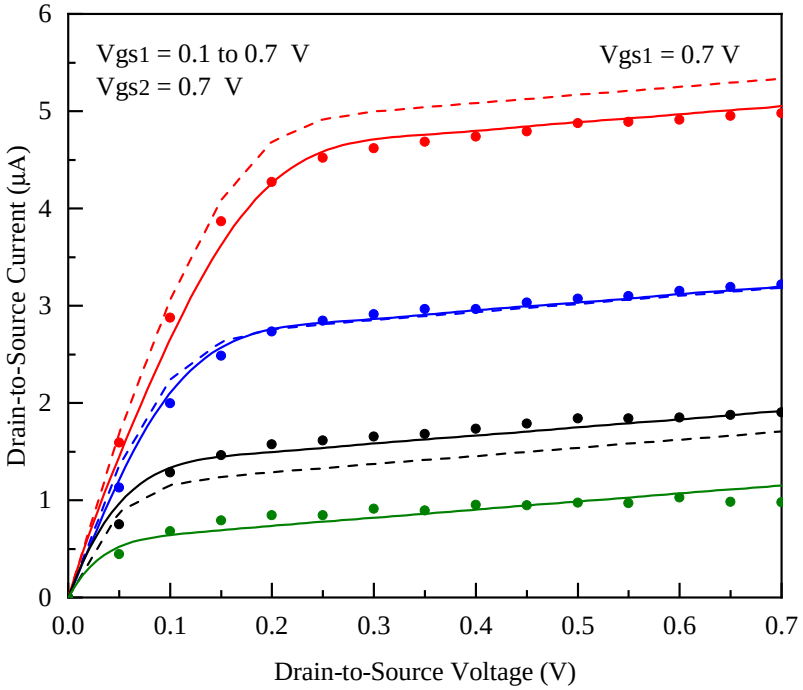

FIGURE 4.4: Comparison between modeled (Solid line: proposed model with the effect of height, Broken line: model without the effect of height [124]) and simulated (Dots) $I-V$ characteristics of an independent gate FinFET with L_g= 10.8 nm.

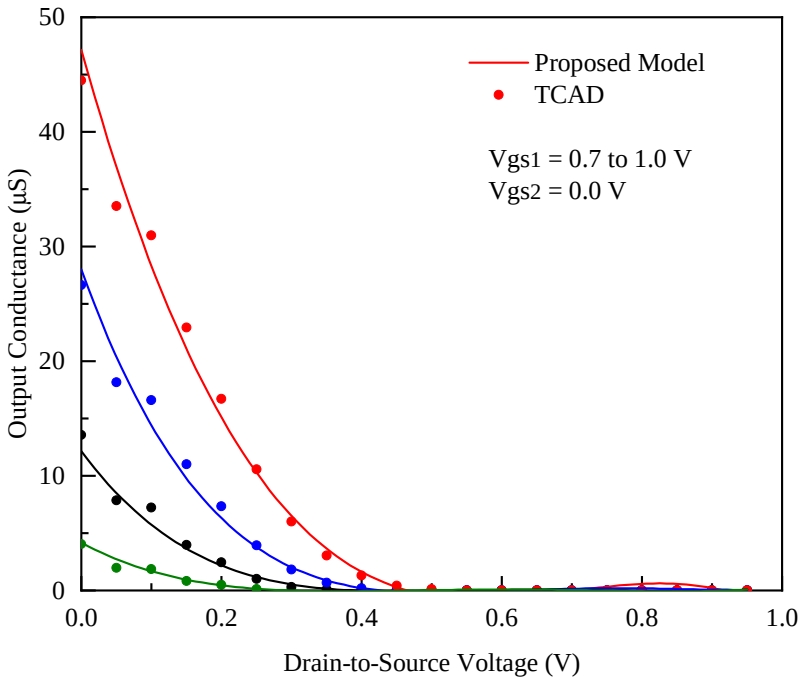

FIGURE 4.5: Comparison between modeled and simulated output characteristics of an independent gate FinFET with L_g= 100 nm.

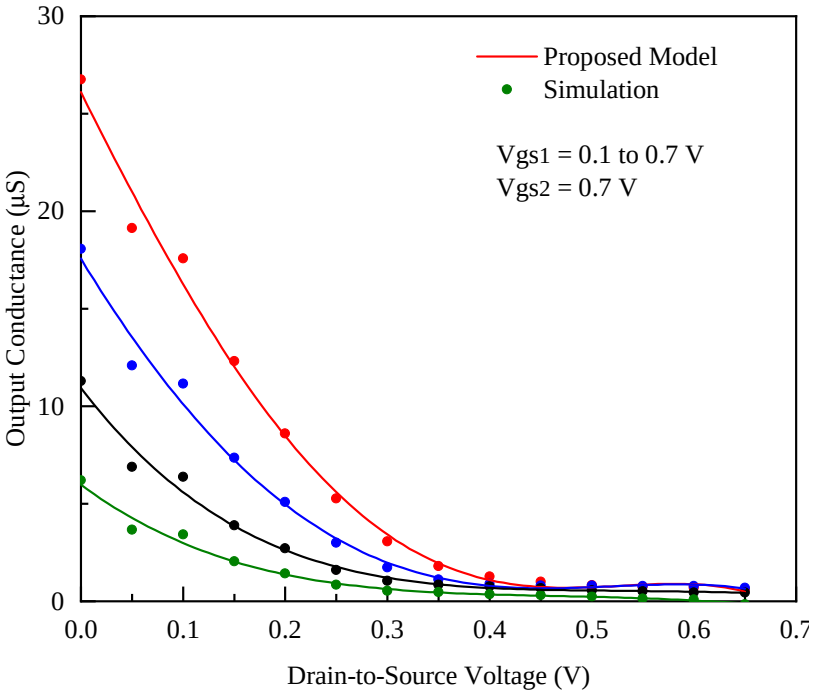

FIGURE 4.6: Comparison between modeled and simulated output characteristics of an independent gate FinFET with L_g= 10.8 nm.

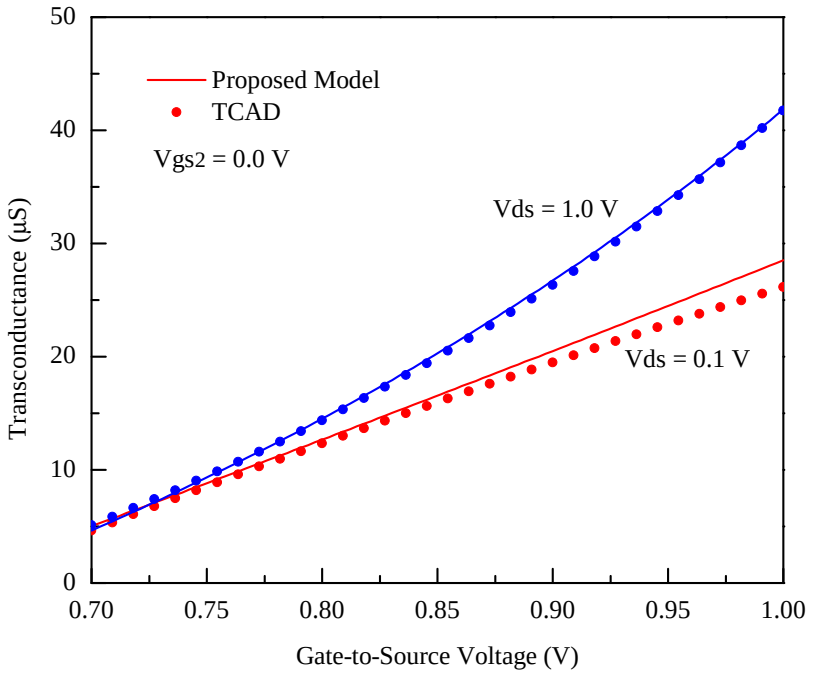

FIGURE 4.7: Comparison between modeled and simulated transfer characteristics of an independent gate FinFET with L_g= 100 nm.

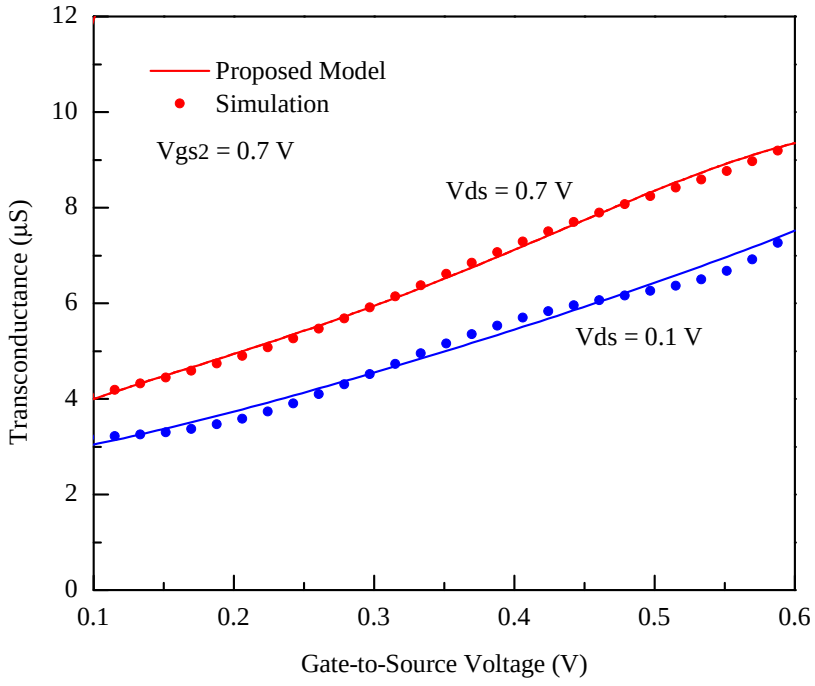

FIGURE 4.8: Comparison between modeled and simulated transfer characteristics of an independent gate FinFET with L_g= 10.8 nm.

To study the response of the model for transfer characteristics, Figs. 4.7 and 4.8 are plotted. The results of the figures show that the model is adequate in predicting the response of the device when the gate voltage is varied. For both linear and saturation regions, the model is equally valid and it also foresees the effect of back gate voltages on the transfer characteristics.

4.4 Summary

In this chapter, an $I-V$ model for independent gate FinFETs is presented. The model uses the potential distribution inside the channel of the FinFET device by solving Poisson's equation with appropriate boundary conditions. The surface potential acquired by the Poisson's equation is used to derive the $I-V$ expression. The model is tested against independent gate FinFETs of varying dimensions, and a good accuracy between the simulated and modeled results show the validity of the proposed model, and its potential use in simulation softwares.

Chapter 5

Heterojunction FinFETs Analytical Model

5.1 Introduction

The downscaling of FET devices is a perpetual pursuit of device shrinkage to meet the growing requirements of the electronic industry. Due to the increase in short channel effects in CMOS devices, the validity of Moore's law is in question [128]. To reduce short channel effects and to meet the ever expanding need of the industry, multi-gate FETs were introduced [129–132]. In contrast to conventional COMS devices, FinFETs have multiple gates acting on the channel which induce more control on the channel with reduced leakage current [49].

In recent years, AlGaN/GaN based FinFETs are taking over the industry due to their superior electrical performance [133, 134]. GaN based devices offer higher mobility, saturation velocity and breakdown voltages [135]. Also, due to the wider bandgap and piezoelectric effect, formation of 2DEG at AlGaN/GaN heterojunction gives a relatively large n_s; facilitating in higher currents at the same bais. Additionally, GaN has low intrinsic carrier concentration at higher temperatures relative to Si [136], which allows GaN based FinFETs to operate reliably at high temperature.

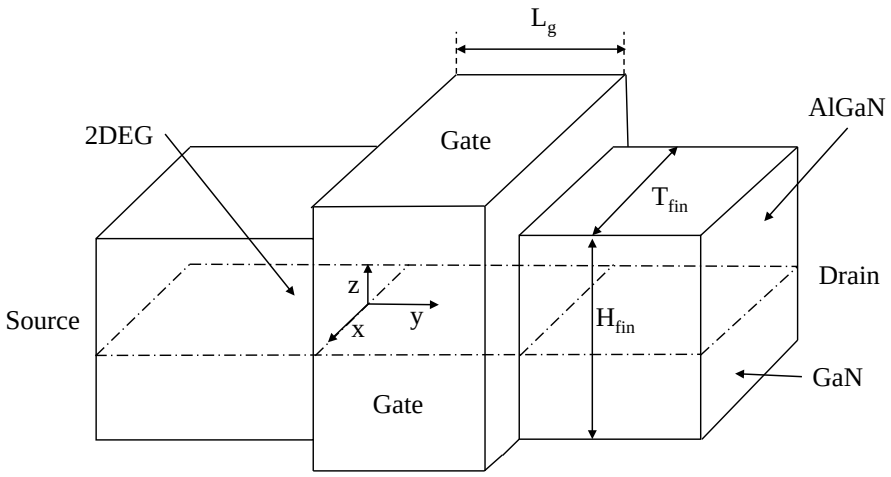

FIGURE 5.1: A view of AlGaN/GaN FinFET channel.

A mathematical model explaining the characteristics of the device involving channel field and device physical parameters, would be a beneficial tool to exploit the device to its full potential. As the gate of a FinFET covers its channel from three directions, as shown in Fig. 5.1, conventional HEMT models cannot by utilized, as they are conceived for devices upon which only one gate acts to control the channel current [137, 138]. On the other hand, FinFET models work on the principle of bulk and/or intrinsic charge concentrations [97, 139] and not on n_s, thus, they are prone to produce error in predicting the characteristics of AlGaN/GaN based FinFETs whose current is controlled by n_s.

In this chapter, an $I-V$ model is developed for AlGaN/GaN FinFETs by solving the potential distribution across 2DEG of the device. 2D Poisson equation is solved to get the potential across the 2DEG plane, which controls n_s. By assessing n_s and its dependence on the applied bais, over the entire channel of the device, $I-V$ expressions for linear and saturation region of an AlGaN/GaN FinFET are obtained. The developed technique is checked for the devices of varying dimensions to validate its accuracy.

5.2 Model Development

2DEG formation between the heterojunction of AlGaN/GaN layers, as illustrated in Fig. 5.1, plays a crucial role in determining the characteristics of a FinFET [140]. The formation of 2DEG defining n_s at the interface of the two layers can be expressed as [141]

$$n_s = \frac{\epsilon_s}{qd}(\psi_{gs} - V_{th} - E_F - \psi_{ds}) \tag{5.1}$$

where a quadratic relationship defined in Ref. [142] links E_F and n_s, and is given by

$$E_F = \gamma_1 + \gamma_2 n_s^{1/2} + \gamma_3 n_s \tag{5.2}$$

The variable V_{th} of Eq. (5.1) may, however, have two distinct definitions. For doped heterostructure layers, it is expressed as [138]

$$V_{th} = \phi_B - \Delta E_c - \frac{qNd^2}{2\epsilon_s} \tag{5.3}$$

whereas, V_{th} of a FinFET, which works on the principle of polarization and have undoped layers, is given by [143]

$$V_{th} = \phi_B - \Delta E_c - \frac{\sigma d}{\epsilon_s} \tag{5.4}$$

The characteristics of a FinFET are determined by the potentials ψ_{gs} and ψ_{ds}, which can be assessed by applying 2D Poisson equation on the device geometry defined in Fig. 5.1. The gate of a FinFET wraps the 2DEG from three sides and can deplete the channel from all the three directions simultaneously. However, this action may not be uniform. Keeping in view the geometry of the device, one can assume that the effectiveness of the side gates will be much greater than the top gate, therefore under this assumption, the spatial variation of the channel potential of an undoped AlGaN/GaN HEMT can be expressed as

$$\frac{\partial \psi^2}{\partial x^2} + \frac{\partial \psi^2}{\partial y^2} = \frac{\sigma d}{\epsilon_s} \tag{5.5}$$

The boundary conditions of Eq. (5.5) are

$$\psi(x,0) = V_s \qquad \psi(x,L_g) = V_d \qquad \psi(T_{fin}/2,y) = V_g \qquad \psi(-T_{fin}/2,y) = V_g \tag{5.6}$$

ψ can be broken into two parts, i.e. $\psi = \psi_1 + \psi_2$; where ψ_1 is the solution of Poisson equation with all boundary conditions equal to zero and ψ_2 is the solution of Laplace equation. Therefore,

$$\frac{\partial \psi_1^2}{\partial x^2} + \frac{\partial \psi_1^2}{\partial y^2} = \frac{\sigma d}{\epsilon_s} \tag{5.7}$$

with boundary conditions

$$\psi_1(x,0) = 0 \qquad \psi_1(x,L_g) = 0 \qquad \psi_1(T_{fin}/2,y) = 0 \qquad \psi_1(-T_{fin}/2,y) = 0 \tag{5.8}$$

Lets consider that $\psi_1 = X_1(x)Y_1(y)$ and by separation of variables, Eq. (5.7) can be expressed as

$$X_1'' - k^2 X_1 = 0 \qquad Y_1'' + k^2 Y_1 = 0 \tag{5.9}$$

Using the boundary conditions given in Eq. (5.8) on Eq. (5.9), one gets

$$X_{1m} = -\sin\frac{(m+1)\pi x}{T_{fin}/2} \qquad Y_{1n} = \sin\frac{(n+1)\pi \acute{y}}{L_g} \qquad m,n = 0,1,2,..... \tag{5.10}$$

where,

$$k = \frac{(m+1)\pi x}{T_{fin}/2} \qquad y = \frac{(n+1)\pi \acute{y}}{L_g}\left(\frac{(m+1)\pi x}{T_{fin}/2}\right)^{-1}$$

So, the general solution of ψ_1 is

$$\psi_1 = -\sum_{m,n=0}^{\infty} C_{1mn} \sin\frac{(m+1)\pi x}{T_{fin}/2} \sin\frac{(n+1)\pi \acute{y}}{L_g} \tag{5.11}$$

Eq. (5.11) satisfies all the boundary conditions given by Eq. (5.8). To find C_{1mn}, substitute Eq. (5.11) in Eq. (5.7)

$$\frac{\sigma d}{\epsilon_s} = \sum_{m,n=0}^{\infty} \left[C_{1mn} \left(\frac{(m+1)^2\pi^2}{T_{fin}^2/4} + \frac{(n+1)^2\pi^2}{L_g^2} \right) \right] \sin \frac{(m+1)\pi x}{T_{fin}/2} \sin \frac{(n+1)\pi \acute{y}}{L_g} \tag{5.12}$$

Now, the term

$$C_{1mn} \left(\frac{(m+1)^2\pi^2}{T_{fin}^2/4} + \frac{(n+1)^2\pi^2}{L_g^2} \right) =$$

$$\frac{\int_0^{T_{fin}/2} \int_0^{L_g} \frac{q\sigma}{\epsilon_s} \sin \frac{(m+1)\pi x}{T_{fin}/2} \sin \frac{(n+1)\pi \acute{y}}{L_g} dx d\acute{y}}{\int_0^{T_{fin}/2} \sin^2 \frac{(m+1)\pi x}{T_{fin}/2} dx \int_0^{L_g} \sin^2 \frac{(n+1)\pi \acute{y}}{L_g} d\acute{y}} \tag{5.13}$$

so,

$$C_{1mn} = \frac{8 \int_0^{T_{fin}/2} \int_0^{L_g} \frac{q\sigma}{\epsilon_s} \sin \frac{(m+1)\pi x}{T_{fin}/2} \sin \frac{(n+1)\pi \acute{y}}{L_g} dx d\acute{y}}{T_{fin} L_g \left(\frac{(m+1)^2\pi^2}{T_{fin}^2/4} + \frac{(n+1)^2\pi^2}{L_g^2} \right)} \tag{5.14}$$

The equation for ψ_2 is

$$\frac{\partial \psi_2^2}{\partial x^2} + \frac{\partial \psi_2^2}{\partial y^2} = 0 \tag{5.15}$$

subjected to boundary conditions

$$\psi_2(x,0) = V_s \qquad \psi_2(x,L_g) = V_d \qquad \psi_2(T_{fin}/2,y) = V_g \qquad \psi_2(-T_{fin}/2,y) = V_g \tag{5.16}$$

The solution of Eq. (5.15) can be written as $\psi_2 = \psi_{21} + \psi_{22} + \psi_{23} + \psi_{24}$, where the boundaries of ψ_{ij} are defined by Fig. 5.2. Considering ψ_{21} and its boundary conditions given in Fig. 5.2, the solution by separation of variables i.e. $\psi_{21} =$

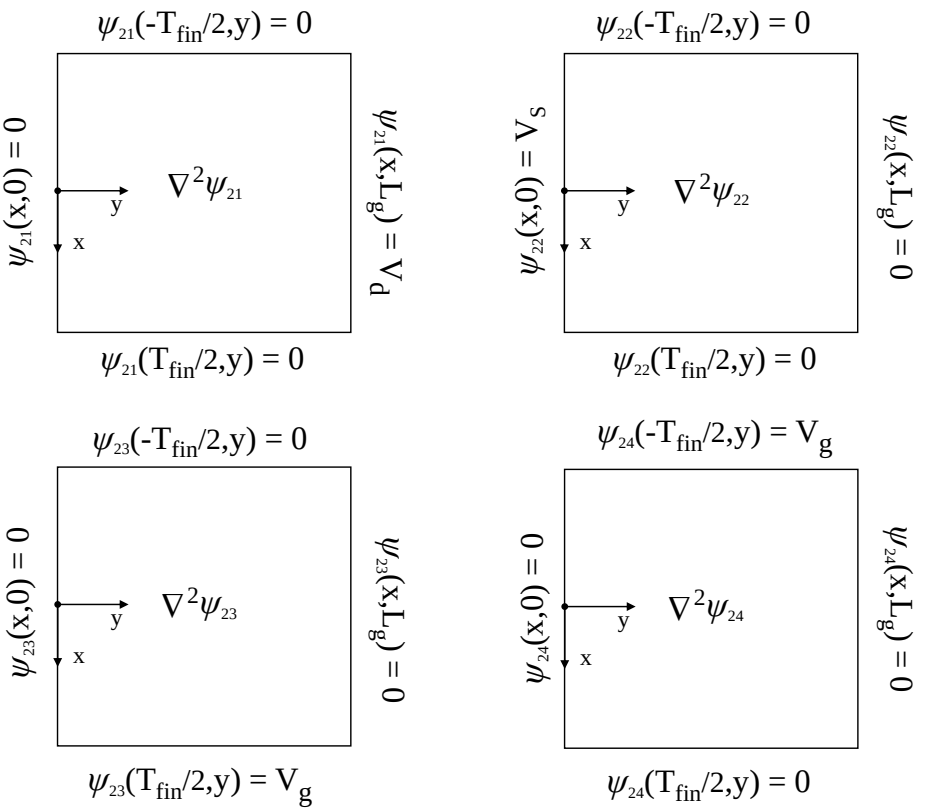

FIGURE 5.2: Boundary conditions of ψ_2 broken into four parts: $\psi_2 = \psi_{21} + \psi_{22} + \psi_{23} + \psi_{24}$.

$X_{21}(x)Y_{21}(\acute{y})$ is

$$X_{21m} = \sin \frac{(m+1)\pi x}{T_{fin}/2} \qquad Y_{21n} = \sinh \frac{(n+1)\pi \acute{y}}{L_g} \qquad m, n = 0, 1, 2, ... \quad (5.17)$$

Thus, the general solution is

$$\psi_{21} = \sum_{m,n=0}^{\infty} C_{21mn} \sin \frac{(m+1)\pi x}{T_{fin}/2} \sinh \frac{(n+1)\pi \acute{y}}{L_g} \quad (5.18)$$

By applying boundary condition $\psi_{21}(x, L_g) = V_d$ on Eq. (5.18), one gets

$$\psi_{21}(x, \acute{y} = L_g) = V_d = \sum_{m,n=0}^{\infty} C_{21mn} \sin \frac{(m+1)\pi x}{T_{fin}/2} \sinh (n+1)\pi \quad (5.19)$$

therefore,

$$C_{21mn} = \frac{4 \int_0^{T_{fin}/2} V_d \sin \frac{(m+1)\pi x}{T_{fin}/2} \, dx}{T_{fin} \sinh (n+1)\pi} \tag{5.20}$$

Similarly, by using the same approach, we get,

$$\psi_{22} = 0 \tag{5.21}$$

$$\psi_{23} = \sum_{m,n=0}^{\infty} C_{23mn} \sinh \frac{(m+1)\pi x}{T_{fin}/2} \sin \frac{(n+1)\pi \acute{y}}{L_g} \tag{5.22}$$

$$\psi_{24} = -\psi_{23} \tag{5.23}$$

and

$$C_{23mn} = \frac{2 \int_0^{L_g} V_g \sin \frac{(n+1)\pi \acute{y}}{L_g} d\acute{y}}{L_g \sinh (m+1)\pi} \tag{5.24}$$

Now, the effective potentials are given as

$$\psi_{ds} = \psi_{21} + \psi_{22} + \psi_1 \qquad \psi_{gs} = |\psi_{23}| + |\psi_{24}| \tag{5.25}$$

By combining Eqs. (5.1) and (5.2), n_s can be written an

$$n_s = \left[\frac{-\gamma_2 + \sqrt{\gamma_2^2 + 4\gamma_4(\psi_{gs} - V_{th} - \psi_{ds} - \gamma_1)}}{2\gamma_4} \right]^2 \tag{5.26}$$

where,

$$\gamma_4 = \gamma_3 + \frac{qd}{\epsilon_s}$$

Eq. (5.26) is plotted for both FinFETs and HEMTs and is shown in Fig. 5.3. For conventional HEMTs, $\psi_{gs} = V_{gs}$, while for FinFETs, the value of ψ_{gs} is given by Eq. (5.25). From the figure, it can be seen that n_s of both the devices is the same when no gate bais is applied and it reduces with the increase in the magnitude of V_{gs}. However, n_s of FinFETs reduce more rapidly and has a greater

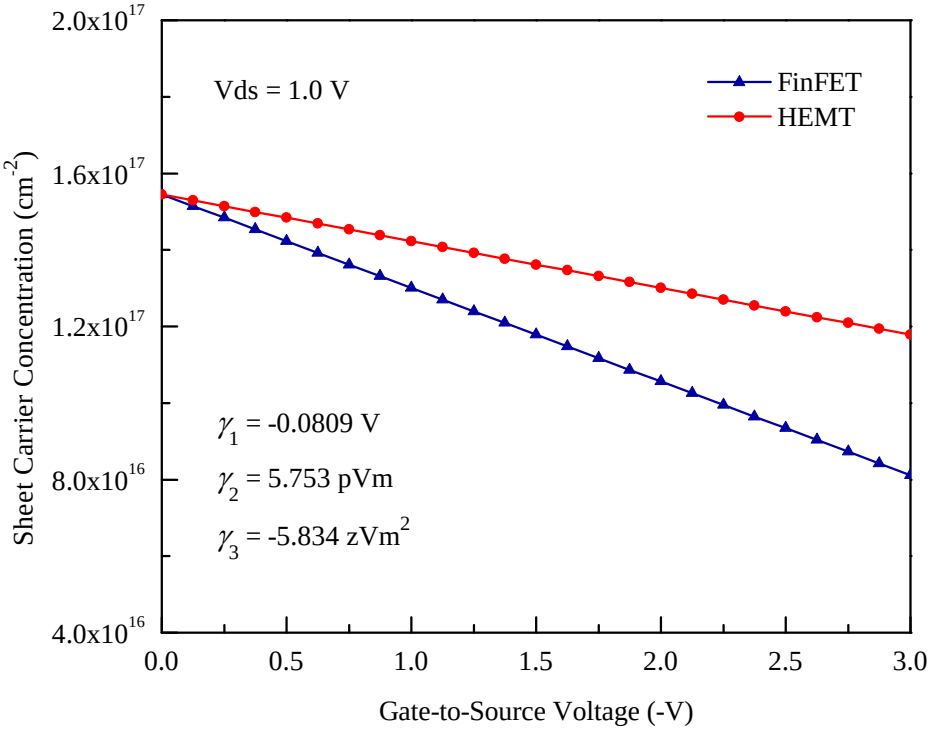

FIGURE 5.3: Sheet carrier concentration attained by Eq. (5.26) for both HEMTs and FinFETs. In the figure, p = $\times 10^{-12}$ and z = $\times 10^{-21}$.

slope compared to HEMTs. This could be associated with the tri-gate structure of the device, where all the three gates deplete n_s at the same time, increasing the effectiveness of V_{gs} on the device.

5.2.1 DC Characteristics

Channel current, I_{ds} of an AlGaN/GaN FinFET can be expressed as

$$I_{ds} = qWn_s v_d \tag{5.27}$$

v_d describes the velocity of the carriers drifting through the channel and it can be expressed as [107]

$$v_d = \begin{cases} \dfrac{\mu_0 E_y}{1 + E_y/2E_{sat}}, & \text{for} \quad E_y = d\psi_{ds}/dy < 2E_{sat} \\ v_{sat}, & \text{for} \quad E_y = d\psi_{ds}/dy > 2E_{sat} \end{cases} \tag{5.28}$$

Combining Eqs. (5.27) and (5.28) and integrating over the entire channel, gives the linear region current

$$I_{ds(lin)} = \frac{2(qWv_{sat})}{\gamma_4(2\psi_L + \psi_{ds})} \int_0^{\psi_{ds}} n_s \, d\psi_{ds} \tag{5.29}$$

where, $\psi_L = E_{sat}L_g$. Using the definition of n_s given in Eq. (5.26) and applying the approximation $[4\gamma_4\psi_{ds} + \gamma_2^2 + 4\gamma_4\psi_{g1}] \approx \gamma_2^2 + 4\gamma_4\psi_{g1}$ as $[4\gamma_4\psi_{ds} << \gamma_2^2 + 4\gamma_4\psi_{g1}]$, one gets

$$I_{ds(lin)} = \frac{\xi(2\psi_{ds}\psi_{g2} - \psi_{ds}^2)}{2\psi_L + \psi_{ds}} \tag{5.30}$$

where,

$$\xi = \frac{qWv_{sat}}{\gamma_4} \tag{5.31}$$

$$\psi_{g2} = 2\psi_{g1} + \frac{\gamma_2^2}{\gamma_4}\left(1 - \frac{2}{3}\sqrt{1 + \frac{4\gamma_4\psi_{g1}}{\gamma_2^2}}\right) \tag{5.32}$$

$$\psi_{g1} = \psi_{gs} - V_{th} - \gamma_1 \tag{5.33}$$

To find the saturation current, first the saturation point must be identified. Eqs. (5.27) and (5.30) are simultaneously solved for $\psi_{ds} = \psi_{ds(sat)}$ to get

$$\psi_{ds(sat)} = \frac{2\psi_{g2}\psi_L}{\psi_{g2} + 2\psi_L} \tag{5.34}$$

and

$$I_{ds(sat)} = \frac{\xi\psi_{g2}}{\psi_{g2} + 2\psi_L} \tag{5.35}$$

After the onset of current saturation, increase in V_{ds} results in the shrinking of the channel and this phenomenon is called channel length modulation. Under these conditions $I_{ds(sat)}$ becomes

$$I_{ds(sat)} = \frac{\xi\psi_{g2}}{\psi_{g2} + 2(\psi_L - E_{sat}\Delta L_g)} \tag{5.36}$$

where, ΔL_g can be determined by some iterative technique [144].

TABLE 5.1: Parameters of AlGaN/GaN FinFETs used in this study. For both the devices, $L_g = 0.5$ μm. In the table $\mu = \times 10^{-6}$, n = $\times 10^{-9}$, p = $\times 10^{-12}$, f = $\times 10^{-15}$ and G = $\times 10^{6}$.

Ref.	T_{fin} (nm)	H_{fin} (nm)	W (μm)	γ_1 (V)	γ_2 (pVm)	γ_3 (fVm^2)	σ (cm^{-2})	v_{sat} (Gms^{-1})	ΔL_g (μm)
T_1 [145]	70	60	17.5	0.01	3.38	964	0.038	0.108	0.004
T_2 [146]	60	50	9	0.07	4.23	0.01	0.088	0.561	0.005

5.3 Results and Discussion

To judge the validity of the developed model, AlGaN/GaN FinFETs of different dimensions were chosen and their details are mentioned in Table 5.1. From the table, it can be seen that both the devices are of submicron dimensions and have similar L_g, while their other dimensions are different. This will provide the model with the challenge to predict the $I - V$ characteristics of FinFETs of varying physical dimensions.

To plot the $I - V$ response of the devices mentioned in Table 5.1, Eqs. (5.30), (5.34) and (5.36) are utilized. Eq. (5.30) simulates the linear region current and Eq. (5.36) is used to predict saturation current of the devices. To know where the saturation current begins with respect to V_{ds}, Eq. (5.34) is utilized. It gives the switching point between the two expressions for a smooth transition between linear and saturation regions.

By engaging the developed expressions, $I - V$ response of devices T_1 and T_2 is plotted and shown in Fig. 5.4. From the figure, it can be observed that in both the devices, the proposed model is successful in predicting the response of the device and the accuracy of the model is also within acceptable margin.

Figure 5.5 is the plot of output characteristics for the devices listed in Table 5.1, which are attained by differentiating Eqs. (5.30) and (5.36) with respect to V_{ds}. From the figure, it can be seen that the model is good enough to predict the change in the device characteristics as V_{ds} increases and the model holds its accuracy for both the regions of operation, i.e. the linear and the saturation region of operation.

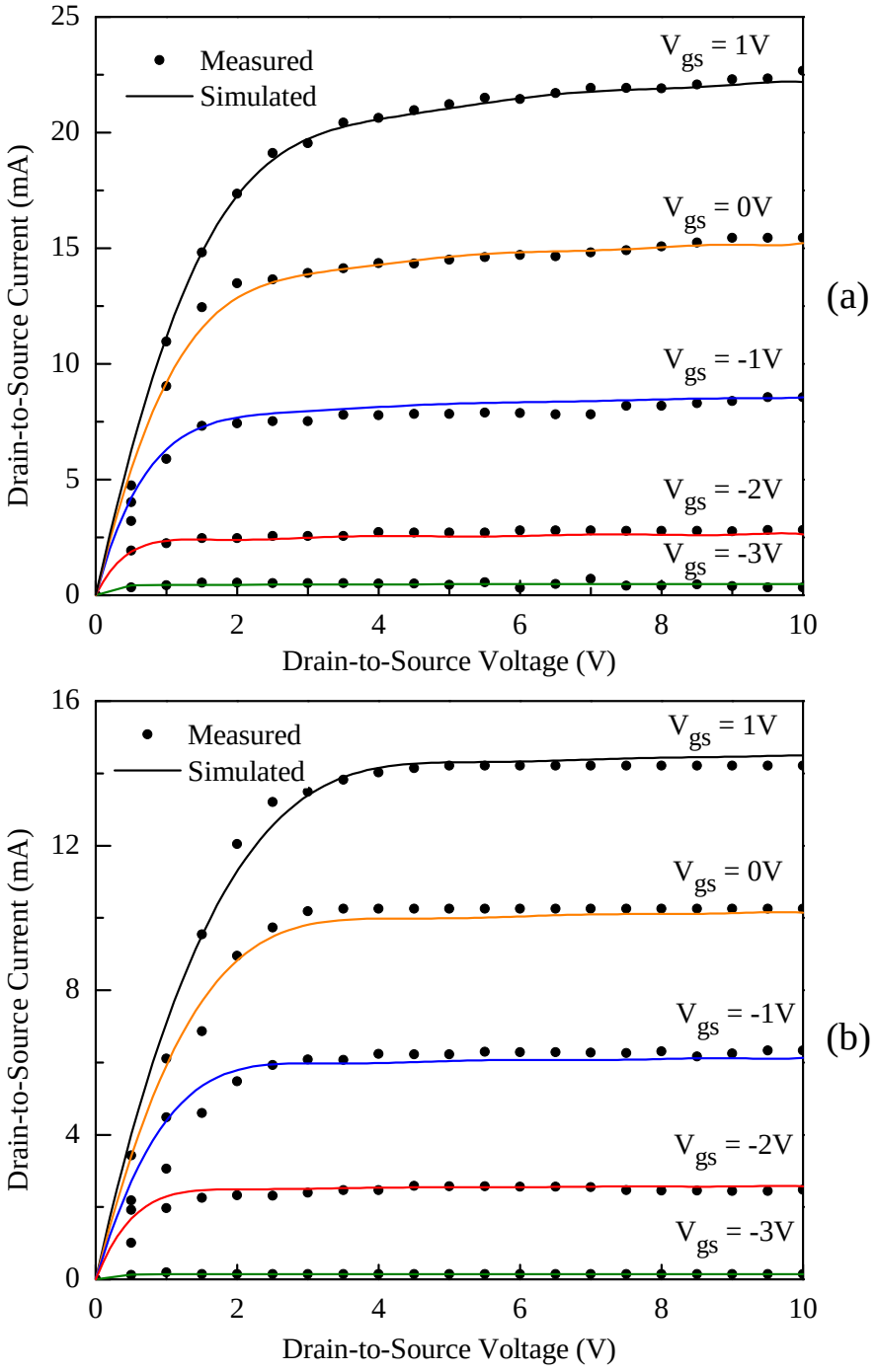

FIGURE 5.4: $I-V$ characteristics of AlGaN/GaN FinFETs: a) $T_{fin} = 70$ nm [145] and b) $T_{fin} = 60$ nm [146].

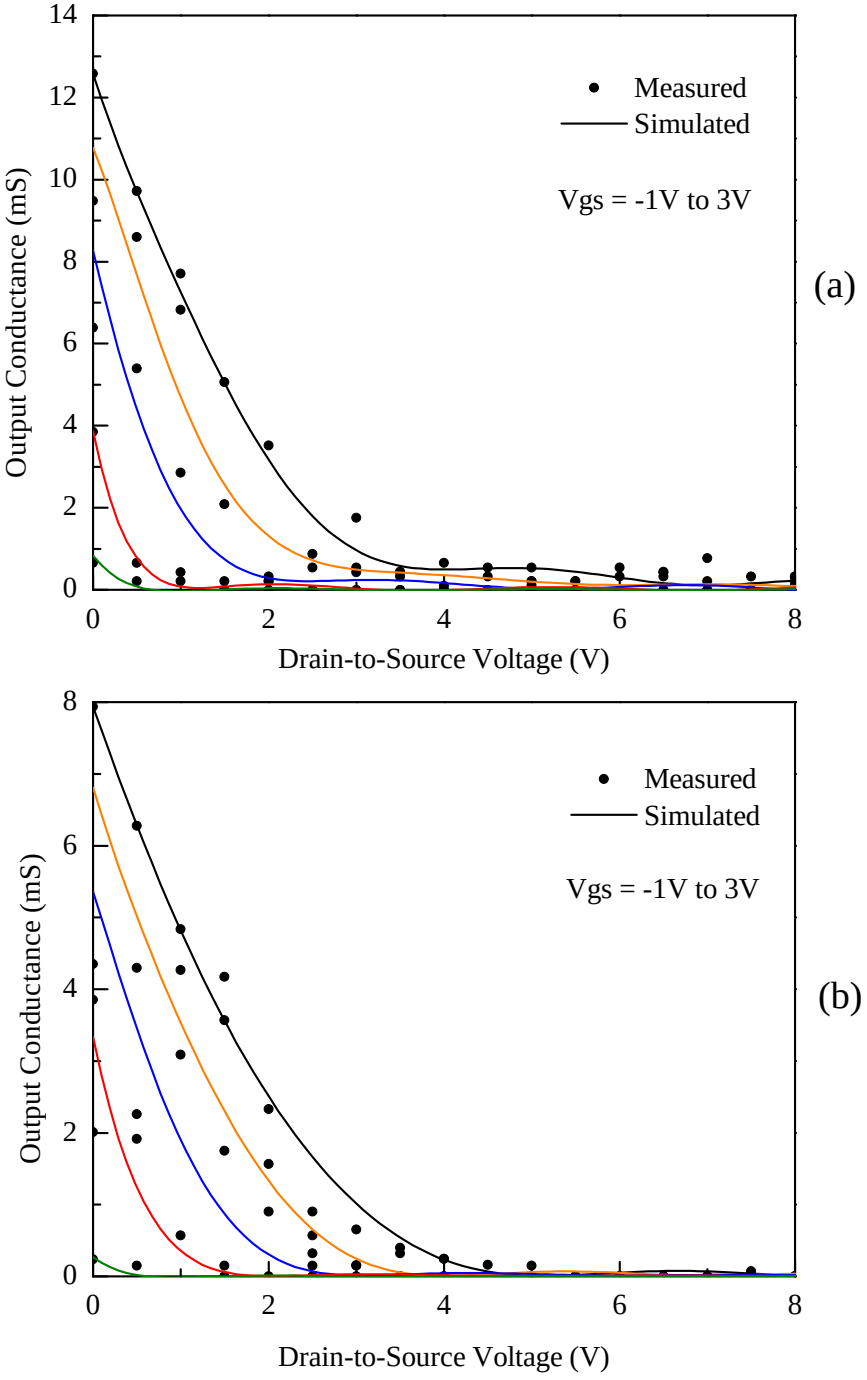

FIGURE 5.5: Output characteristics of AlGaN/GaN FinFETs: a) $T_{fin} = 70$ nm [145] and b) $T_{fin} = 60$ nm [146].

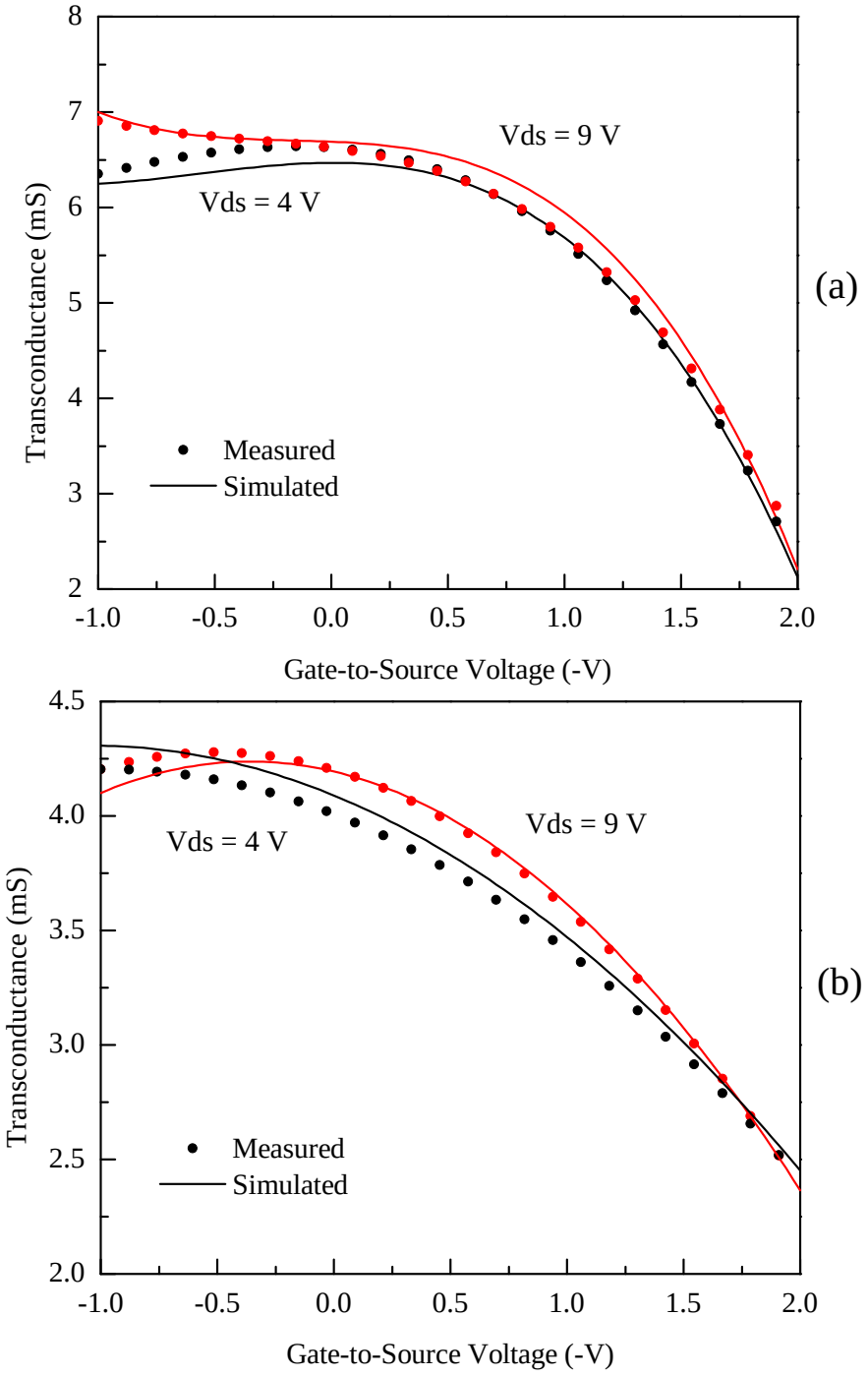

FIGURE 5.6: Transfer characteristics of AlGaN/GaN FinFETs: a) $T_{fin} = 70$ nm [145] and b) $T_{fin} = 60$ nm [146].

Figure 5.6 is plotted by differentiating Eqs. (5.30) and (5.36) with respect to V_{gs}, to get the transfer characteristics. Both the figures show an almost ideal device behavior, i.e. the peak of the curve is observed at higher V_{gs} and it decreases with the decrease in V_{gs} at almost a constant rate. The proposed model also follows the trend of the experimental data with a good degree of accuracy in both the linear as well as in the saturation regions of operation. Hence, in a nutshell, it can be said the proposed model is accurate enough to predict $I-V$ characteristics of AlGaN/GaN FinFETs.

5.4 Summary

In this chapter, an analytical model is developed to predict $I-V$ characteristics of AlGaN/GaN FinFETs. The model includes the effect of tri-gate geometry on the n_s of the device by utilizing a 2D Poisson equation with appropriate boundary conditions. It has been shown that n_s of FinFETs deplete at a faster rate relative to conventional HEMTs, because of the side gates present in the device. By utilizing the expression of n_s, the $I-V$ model is developed for both linear and saturation regions of operation. The model is tested on devices with varying physical dimensions and the results show that the proposed model is fairly accurate for both the regions of operation and can be utilized in predicting the response of AlGaN/GaN FinFETs.

Chapter 6

A Compact Mobility Based FinFETs $I-V$ Model

6.1 Introduction

To cope with the advancing needs of the electronic industry, device shrinkage was carried out successfully till the 1990s [147]. A further decrease in the size of the device revealed non ideal device behavior referred to as short channel effects [148]. To cater these effects and continue the scaling of the devices, multi-gate FinFETs were introduced [6, 9, 77, 149]. These devices contrary to conventional FETs offer better gate control upon the channel and have reduced the sealing effect of devices for high-end applications.

FinFET is a 3D device in which the gate of the device envelopes the channel from all the three sides. This provides the gate, extra control on the device and the short channel effects are lowered [132, 150, 151]. Figure 6.1 shows the general structure of a FinFET. As stated earlier, it can be seen from the figure that the channel is completely covered by the gate of the device. This allows the gate 3D control on the channel and reduces the leakage current of the device to a significant level [95].

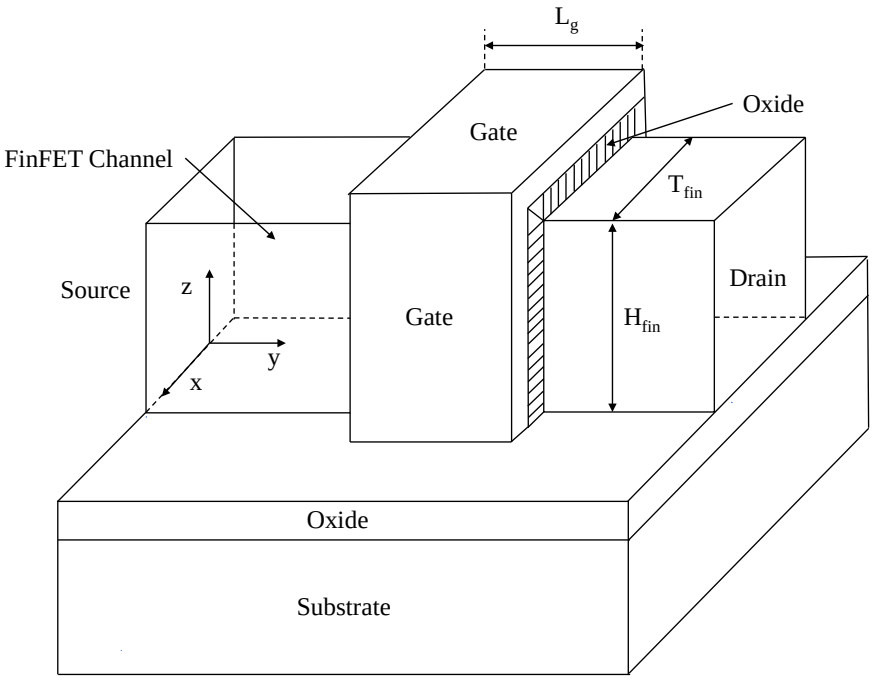

FIGURE 6.1: General structure of a tri-gate FinFET.

A mathematical model is a prerequisite for full understanding of an electronic device, especially for its integration into electrical circuitries. To fully understand the workings of FinFETs, device modeling is required. There are quite a large number of models present in the literature for the simulation of FinFET characteristics [73, 152–154]. Generally, these models employ Poisson's equation, superposition principle, Green's function and power series expansion. As a result, these models are quite complex in nature and are difficult to handle from a design engineer's perspective.

It is an established fact that the characteristics of a FinFET are controlled by its physical dimensions, which in turn determine μ of carriers drifting inside the channel [155]. The μ follows a non-linear profile which depends upon the channel field defined by the applied V_{gs} and V_{ds} potentials [156]. By increasing the field, there is a rise in the magnitude of μ which then attains its saturation value [157]. This phenomenon plays a prime role in determining the $I-V$ characteristics of FinFETs. Thus, an accurate assessment of mobility is of crucial importance in device modeling.

In this chapter, a compact model for CAD is presented, which utilizes the change

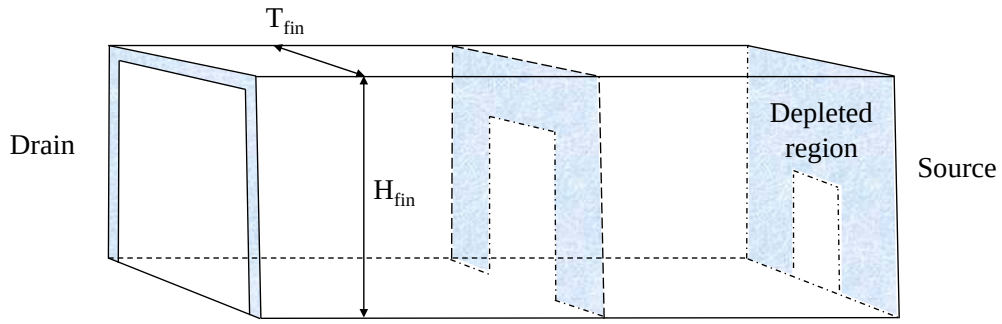

FIGURE 6.2: A zoomed view of a biased tri-gate FinFET channel.

in μ to predict the $I-V$ response of a FinFET. The model is quite compact in nature and can easily be employed in CAD software meant for device modeling. According to our conservative estimate; there is no such model reported in the literature thus, the proposed model could be a useful tool to exploit the device fullest potential in electronic circuitries.

6.2 Model Development

A tri-gate FinFET device has a 3D channel as illustrated by Fig. 6.2. In this figure a zoomed view of that portion of the device is shown which is covered by the gate metal. This region has got two ends; one towards the drain side and the other towards the source side of the device. Because of the potential difference, there is a non-uniform depletion distribution across the crossection of the channel as evident from Fig. 6.2. Near to the drain side, the depletion layer is of minimum thickness, and this thickness is progressively increasing while moving towards the source side of the device. Thus, the carriers trying to transverse the channel will experience an increasing E, which will effect the value of μ. At higher E, there would be more scattering resulting into the saturation of μ and this effect can be modeled as

$$\beta\frac{d\mu}{dV_{ds}}+\beta^2\mu=\beta^2\mu_G \tag{6.1}$$

where, β describes the slope of μ at relatively low E. At relatively higher E, variable μ attains its maximum value, μ_G, which depends upon V_{gs} and is given by [107]

$$\mu_G = \frac{\mu_0}{1 + \gamma(V_{gs} - V_{th})^{\lambda}} \tag{6.2}$$

where, γ and λ relate μ_0 to μ_G. Considering the fundamental MOSFET configuration, V_{th} of Eq. (6.2) is given by [106]

$$V_{th} = V_{fb} + 2V_m + \frac{qN_b x_{dep}}{C_{ox}} \tag{6.3}$$

where, $V_m = k_B T/q \times \ln(N_b/n_i)$. The value of V_{th} may have a nominal modification dependent upon the geometry and dimensions of the fin [158]. As stated earlier, rate of scattering will increase with increasing E, and as a result, a deceleration of carries could occur. Under such circumstances, the μ profile might not fully comply to Eq. (6.1). To accommodate such 2$^{\text{nd}}$ order effects, Eq. (6.1) is modified as

$$\frac{d^2\mu}{dV_{ds}^2} + 2\beta\frac{d\mu}{dV_{ds}} + \beta^2\mu = \beta^2\mu_G \tag{6.4}$$

Eq. (6.4) describes the change in μ with both V_{ds} and V_{gs}. Figure 6.3 is plotted using Eqs. (6.1) and (6.4). From the figure, it can be seen that initially, μ is very small and by increasing V_{ds}, a linear increase in μ is observed which then saturates to μ_G. From the figure it is obvious that the slope of linear region of Eq. (6.4) is smaller compared to that of Eq. (6.1). This could be associated with the second order effects which might be observed by the scattering of carriers at relatively higher E. The general solution of Eq. (6.4) with initial conditions $\mu(0) = 0$ and $d\mu/dV_{ds}|_{\mu(0)} = 0$, is given by

$$\mu = \mu_G(1 - e^{-\beta V_{ds}} - \beta V_{ds} e^{-\beta V_{ds}}) \tag{6.5}$$

As FinFET is an extension of MOSFET based devices, its channel current, I_{ds} for $V_{gs} > V_{th}$ can be expressed as [159]

$$I_{ds} = \frac{W}{L_g} C_{ox} \mu V_{ds}(V_{gs} - V_{th}) \tag{6.6}$$

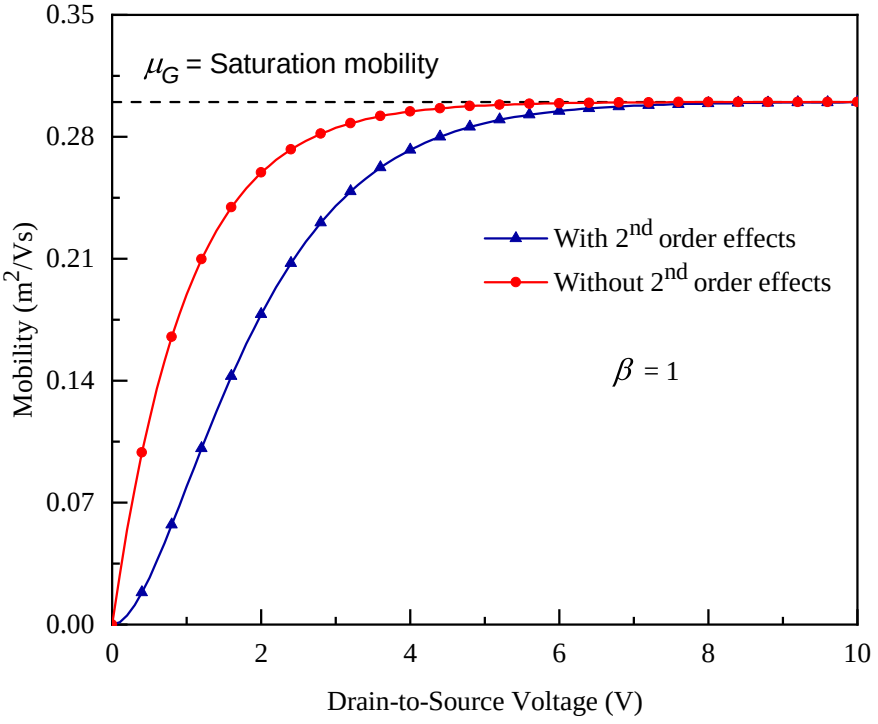

FIGURE 6.3: Mobility profile with [Eq. (6.4)] and without [Eq. (6.1)] second order effects.

where W is the gate width and L_g is the gate length of the device, respectively. Eq. (6.6) represents minimum current at $V_{gs} = V_{th}$, and an increase in the value of V_{gs} will increase I_{ds}. However, there could be non idealities present at the Schottky junction of the FinFET, which can consume a finite magnitude of applied V_{gs}. Furthermore, a finite conductance is usually observed in FinFETs after the onset of current saturation, which will make V_{th} dependent upon V_{ds}. To accommodate these effects Eq. (6.6) is modified

$$I_{ds} = \frac{W}{L_g} C_{ox} \mu V_{ds} (V_{gs} - V_{th}) \left(1 + \frac{\eta V_{gs}}{V_{th} + \alpha V_{ds}}\right) \tag{6.7}$$

where, η controls the effectiveness of V_{gs} and α controls the dependence of V_{th} on the applied V_{ds}. Eq. (6.7) is the final I_{ds} expression which can model the $I-V$ characteristics of FinFETs by involving device physical parameters and bias potentials.

For the sake of completeness g_d and g_m of a FinFET can be found by differentiating I_{ds} with respect of V_{ds} and V_{gs}, respectively, and are given by

$$g_d = \frac{S_3 W C_{ox} V_{ds}(V_{gs}-V_{th})\beta\mu_0 e^{-\beta V_{ds}}}{S_1} + \frac{S_2 W C_{ox} V_{ds}(V_{gs}-V_{th})\alpha\eta\mu_0}{S_1(V_{th}+\alpha V_{ds})^2} - \frac{S_2 S_3 W C_{ox} V_{gs}(V_{gs}-V_{th})}{S_1} \tag{6.8}$$

and

$$g_m = \frac{S_2 S_3 W C_{ox} V_{ds} V_{gs}\gamma\lambda\mu_0(V_{gs}-V_{th})^{\lambda}}{S_1} - \frac{S_2 W C_{ox} V_{ds}(V_{gs}-V_{th})\eta\mu_0}{S_1} - \frac{S_3 S_2 W C_{ox} V_{ds}\mu_0}{S_1} \tag{6.9}$$

where,

$$S_1 = L_g[1+\gamma(V_{gs}-V_{th})^{\lambda}]$$

$$S_2 = -(1-e^{-\beta V_{ds}} - \beta V_{ds} e^{-\beta V_{ds}})$$

$$S_3 = 1 + \frac{\eta V_{gs}}{V_{th}+\alpha V_{ds}}$$

6.3 Parameter Extraction

Particle swarm optimization (PSO) method is used to find the optimum model parameters [160]. Apart from the physical dimensions, I_{ds} is also a function of model parameters and can be expressed as $I_{ds(\mathrm{mod})}(\alpha,\beta,\gamma,\eta,\lambda)$. An $n\times m$ dimensional matrix $P_{ij}[l]$ is initialized with random values and each entity of the matrix is the position of a particle and each particle represents a model parameter. The matrix P_{ij} contains n number of particles and m number of particle batches.

A velocity vector, V_j is also initialized and it contains the maximum velocity of each particle batch. At any instant, $V_j[l]$ can be found as

$$V_j[l] = \frac{max(P_{:j}) - min(P_{:j})}{2} \tag{6.10}$$

At each iteration, $I_{ds(\mathrm{mod})}$ is calculated and compared with the experimental current, $I_{ds(\mathrm{exp})}$ using the objective function

$$E_r = \sqrt{\sum_{Q=R}^{N}\left\{\sum_{P=S}^{M}\left(I_{ds(\mathrm{exp})}^{P,Q} - I_{ds(\mathrm{mod})}^{P,Q}\right)^2\right\} \Big/ \sum_{P=S}^{M} I_{ds(\mathrm{exp})}^{P,Q}} \tag{6.11}$$

where, P and Q are the vectors of V_{ds} and V_{gs}, respectively. V_{ds} has the maximum value N and minimum value R, while V_{gs} has the maximum value M and minimum value S. A minimum tolerance T_{min} is set and during each iteration; ϵ is compared with T_{min} to check the stop criterion; otherwise, the PSO will stop when maximum number of iterations, l_{max} is reached.

The particles with minimum E_r are stacked in local best matrix, $P_{\mathrm{B}}[l]$ and Eq. (6.11) is once again utilized to find the global best matrix, $P_{\mathrm{G}}[l]$. After each iteration, both the position and velocity vectors are updated

$$V_j[l+1] = V_j[l] + \Upsilon V_j[l] \tag{6.12}$$

and

$$P_{ij}[l+1] = P_{ij}[l] + \Upsilon P_{ij}[l] \tag{6.13}$$

$\Upsilon V_j[l]$ and $\Upsilon P_{ij}[l]$ are the learning rates of Eqs. (6.12) and (6.13) given by

$$\Upsilon P_{ij}[l] = \kappa\{P_{ij}[l-1] + f_1(P_{\mathrm{B}}[l] - P_{ij}[l]) + f_2(P_{\mathrm{G}}[l] - P_{ij}[l])\} \tag{6.14}$$

and

$$\Upsilon V_j[l] = \kappa\{V_j[l-1]\} \tag{6.15}$$

f_1 and f_2 of Eq. (6.14) are given as

$$f_1 = f_{max(1)} + \frac{f_{max(1)} - f_{min(1)}}{k_{max}}(l_{max} - l), \tag{6.16}$$

$$f_2 = f_{max(2)} + \frac{f_{max(2)} - f_{min(2)}}{k_{max}}(l_{max} - l), \tag{6.17}$$

TABLE 6.1: Physical parameters of different FinFETs used in this study.

Ref.	Material	L_g (μm)	T_{fin} (nm)	H_{fin} (nm)	W (nm)	V_{th} (V)
T_1 [110]	Si	0.05	10	70	10	-0.01
T_2 [161]	AlGaN/GaN	1.0	80	120	80	-10.5
T_3 [161]	AlGaN/GaN	1.0	140	120	140	-11.0
T_4 [161]	GaN	1.0	60	120	300	-10.5

TABLE 6.2: Extracted parameters for the simulation of $I-V$ characteristics of different FinFET.

Ref.	μ_0 (cm^2/Vs)	γ (1/V)	β(1/V)	λ	η	α
T_1 [110]	354	1.477	3.823	5.923	4.429	0.060
T_2 [161]	1171	1.611	3.729	0.325	1.694	4.886
T_3 [161]	1113	1.694	2.549	0.761	9.14	8.692
T_4 [161]	541	0.188	3.281	2.898	1.042	3.059

where, f_{max} and f_{min} are the maximum and minimum values of f_1 and f_2, respectively. κ in Eq. (6.14) controls the convergence and forces the particles to acquire their equilibrium point by making sure that the overall energy of the system is always decreasing and thus, the particles are always inching closer to their respective equilibrium points.

6.4 Results and Discussion

To check the validity of the proposed $I-V$ model, a number of FinFETs of varying dimensions were selected whose details are listed in Table 6.1. As seen from the table, the devices are fabricated using different channel materials. This will provide a good challenge for the model to establish its validity across numerous materials used in FinFETs technology. The varying dimensions of the devices will also help in judging the model's validity in predicting the $I-V$ characteristics when the device physical parameters are changing.

To find the $I-V$ characteristics, first the model parameters must be extracted. The extraction technique mentioned earlier is employed wherein, to extract model

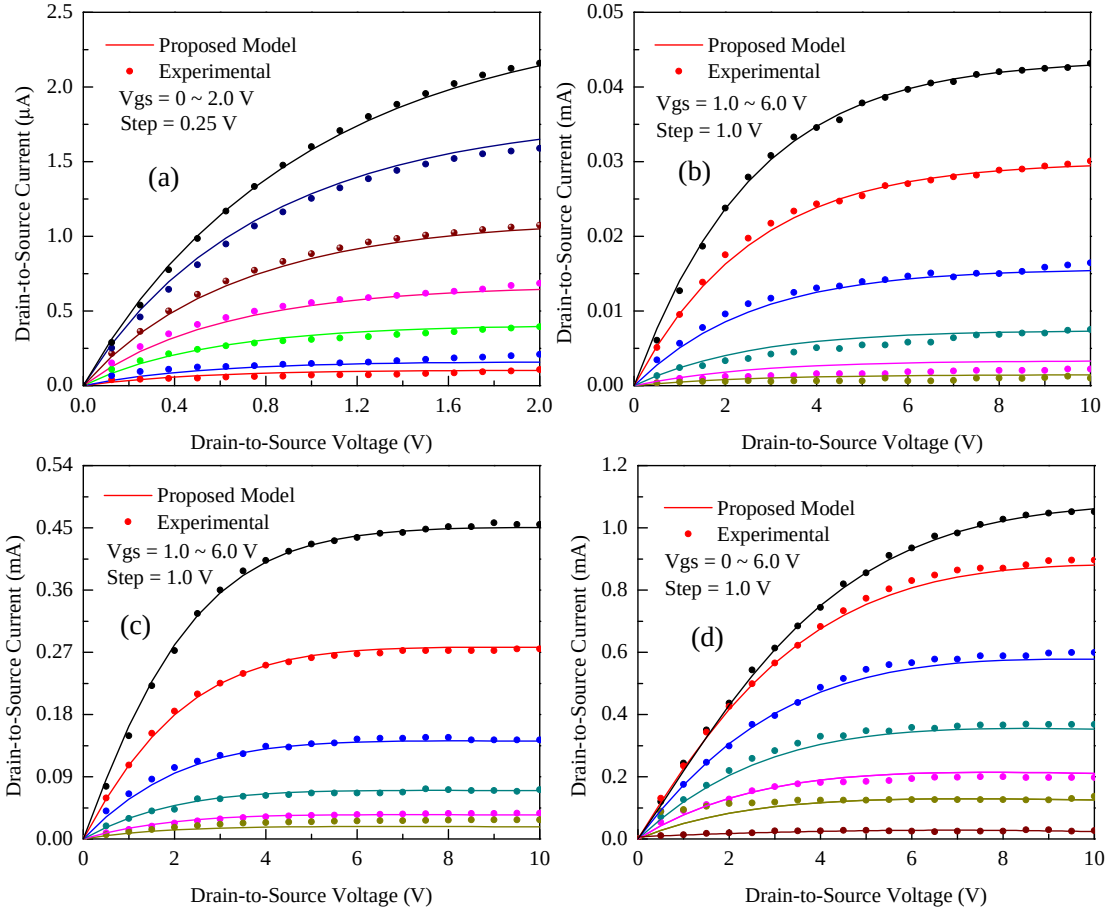

FIGURE 6.4: Experimental and modeled $I-V$ characteristics of FinFETs: (a) $L_g = 0.05$ μm, $W = 140$ μm [110] (b) $L_g = 1$ μm, $W = 80$ μm [161] (c) $L_g = 1$ μm, $W = 140$ μm [161] and (d) $L_g = 1$ μm, $W = 300$ μm [161].

parameters $I_{ds(\mathrm{mod})}$ and $I_{ds(\mathrm{exp})}$ are compared through Eq. (6.11) and the disparity between them is minimized. By using the data of Table 6.1 and Eq. (6.7), parameters of all the four selected devices are extracted and are mentioned in Table 6.2.

Figure 6.4 is plotted using Eq. (6.7) and the parameters extracted and reported in Table 6.2. Figure 6.4a gives the comparison of the experimental data with the proposed model of a Si FinFET. Examination of the figure shows that there is a good agreement between the modeled and the experimental data. It is also seen from the plot of Fig. 6.4a that due to relatively smaller dimensions of the device ($L_g = 50$ nm), the curves follow a more linear path with increasing V_{ds} relative to other plots of Fig. 6.4. This is so, because the V_{ds} bias in this case is only 2 V,

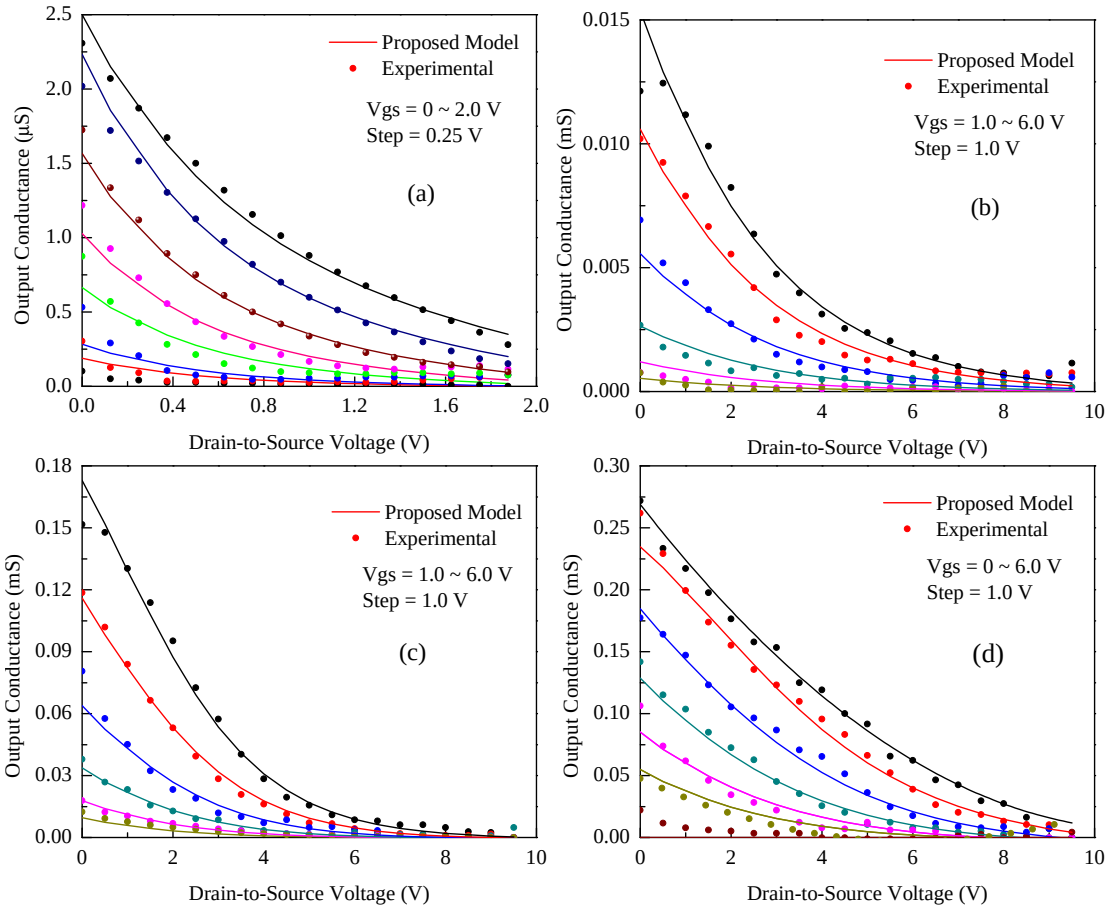

FIGURE 6.5: Experimental and modeled output conductance of FinFETs: (a) $L_g = 0.05$ μm, $W = 140$ μm [110] (b) $L_g = 1$ μm, $W = 80$ μm [161] (c) $L_g = 1$ μm, $W = 140$ μm [161] and (d) $L_g = 1$ μm, $W = 300$ μm [161].

relative to all other devices whose characteristics are sketched on the same scale up to $V_{ds} = 10$ V.

Figure 6.4b shows the $I-V$ characteristics of an AlGaN/GaN FinFET. This device offers ∼2 times higher current relative to the device of Fig. 6.4a at the same drain and source bias. A good agreement is once again observed between the modeled and experimental data, which suggests that the proposed model has the ability to predict $I-V$ characteristics of FinFETs fabricated using different materials and also of different dimensions.

Plots shown in Fig. 6.4c and 6.4d show the $I-V$ characteristics of two FinFETs having $L_g = 1.0$ μm, $W = 140$ μm and $L_g = 1.0$ μm, $W = 300$ μm, respectively. The device having $W = 140$ μm is fabricated using heterojunction material i.e.

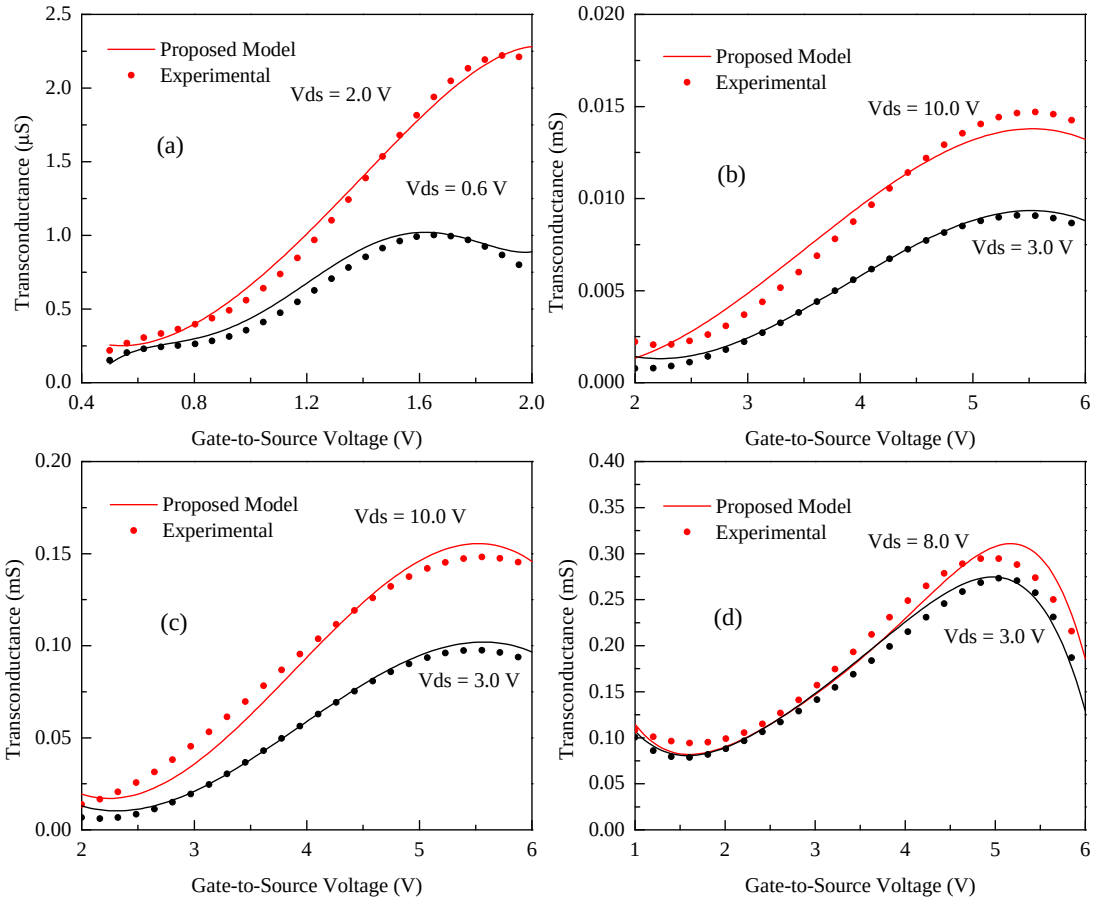

FIGURE 6.6: Experimental and modeled transfer characteristics of FinFETs: (a) $L_g = 0.05$ μm, $W = 140$ μm [110] (b) $L_g = 1$ μm, $W = 80$ μm [161] (c) $L_g = 1$ μm, $W = 140$ μm [161] and (d) $L_g = 1$ μm, $W = 300$ μm [161].

AlGaN/GaN whilst the device of $W = 300$ μm has the channel defined by GaN. The plots of Fig. 6.4c,d exhibit that the model given by Eq. (6.7) holds its accuracy for the devices having different nature and W. Furthermore, Fig. 6.4c represents almost ideal $I-V$ characteristics, wherein the device I_{ds} increases more effectively at higher values of V_{gs}, which is a usual behavior of a FET device [162]. However, this response is not fully observed in the characteristics shown in Fig. 6.4d. But the modeled data in both the cases show good agreement for both the devices; confirming the validity of Eq. (6.7) for FinFETs exhibiting 2^{nd} order effects in their characteristics.

Figure 6.5 gives the output conductance of all the four devices (T_1-T_4), which is plotted using Eq. (6.8). At every V_{gs} and V_{ds} value, the modeled characteristics

are in a reasonable compliance with the experimental data, both in linear and saturation region of operations.

Figure 6.6 shows transfer characteristics of the devices under discussion. These results are attained by using Eq. (6.9), which once again, exhibit a good agreement between experimental and modeled data. In a nutshell, one can conclude that the proposed technique is strong enough to predict the $I-V$ and transfer characteristics of FinFETs, irrespective of their nature and dimensions.

6.5 Summary

In this chapter, a mobility model has been developed to predict the $I-V$ characteristics of FinFETs. The model incorporates the effect of applied potentials on the carriers mobility, which is then used to assess the output and transfer characteristics of FinFETs. Particle swarm optimization has been employed to attain optimum values of the model parameters. Devices of various fabrication material and physical dimensions were selected to test the accuracy of the proposed model. The proposed model has been applied on the devices having gate length $0.05-1$ μm and gate width $10-300$ nm, and a good accuracy has been observed for all the chosen devices. It has been demonstrated that the model can predict the output and transfer characteristics of FinFETs irrespective of the their dimensions and fabrication material.

Chapter 7

Conclusion and Future Works

In modern electronics, MESFETs and HEMTs were the protagonists of the semiconductor industry. To ensure the daily growing need for improvement, smaller semiconductor devices were necessary. However, the scalability of these conventional devices beyond nanometer regime proved to be complicated as short channel effects hampered further device reduction. To overcome these challenges, multi-finger FETs were introduced. Although, multi-finger FETs, as evident from their nomenclature, have multiple gates, but they are controlled by a single electrode. Multi-finger FETs offer low gate resistance without compromising on channel current technology therefore, they are preferred in low noise applications.

Though multi-finger FETs reduce the gate resistance and hence improve the low-noise applications of the device, yet they could not provide an efficient solution to short channel effects, frequently observed in such devices. This is owing to the fact that multi-finger FETs divide the total gate width into multiple strips but their action on the channel remain planer. To overcome this effect, FinFETs are introduced where contrary to planer FETs, gate action on the channel current is from three distinct directions hence, generating more effective control of the Schottky barrier gate on the channel current resulting into considerably reduced short channel effects of the device.

FinFETs can further be divided into two types according to the applied gate potential. If the gate is controlled by a single potential, then the device is called single gate FinFET, on the other hand, if two independent potentials are applied to a segmented gate, then the device is referred to as independent gate FinFET. In both of the FinFETs, the gate controls the channel from three different sides of the fin.

Channel current is of great importance while designing the fabrication parameters of a FET. So, in order to find current flowing through a short gate FinFET, an $I-V$ model is developed and is presented in the 1^{st} part of the thesis. The model is formulated by finding the potential distribution inside the channel of a FinFET. While evaluating the channel potential, 3D structure of a FinFET is taken into consideration. It is an established fact that the geometry of the channel plays an important role in determining the output characteristics of a FinFET. A 3D Poisson equation is, therefore, solved to find the potential distribution inside the channel of the device. By using the channel potential, an $I-V$ model is presented which can predict the output characteristics of nm-FinFETs. It is shown that by adding the third dimension to the Poisson equation, the accuracy of the model is improved, which leads to improved $I-V$ characteristics. Devices of various dimensions are selected to test the validity of the proposed technique and $6-45\%$ improvement is observed in predicting the $I-V$ characteristics of FinFETs with respect to the best reported model in the literature.

In the 2^{nd} part of the thesis, an $I-V$ model for independent gate FinFETs is presented. Poisson's equation is utilized to find the potential distribution inside the channel by adding the effect of channel height. It has been shown that the channel height of the device plays an important role in determining the surface potential, especially, when the device is also under the influence of the voltage applied at the gate sitting at the top of the fin. By involving the surface potential, and by assessing the charge accumulation caused by drain and source potentials, an $I-V$ model is developed. The developed model can find the device current both for the linear as well as the saturation regions of operation. The model is tested on devices of different dimensions and a good agreement between modeled

and simulated results is observed, which validates the authenticity of the proposed model for predicting the DC response of independent gate FinFETs.

To push the FinFET technology a step further, AlGaN/GaN FinFETs were introduced. These devices had better current density and were able to operate at higher temperatures, relative to other FinFETs, due to relatively wider bandgaps of the materials used in their fabrication. FinFET models based on the bulk charges, by their very definition, could not be employed on heterojunction FinFETs, because of the formation of 2DEG, which primarily is responsible for controlling the magnitude of channel current of such devices.

So, as a 3rd part of this research, an analytical model is developed to predict the $I-V$ characteristics of AlGaN/GaN FinFETs. The model includes the effect of tri-gate geometry on the sheet charge concentration of the device by utilizing a 2D Poisson equation with appropriate boundary conditions. It has been observed that the sheet charge density of a modulation doped FinFET depletes faster, relative to conventional HEMTs, because of the two side gates. It has been demonstrated that the developed heterojunction FinFET model is capable of predicting $I-V$ characteristics both for the linear as well as for the saturation regions of operation. The heterojunction FinFET model has been tested on devices of varying physical dimensions and the results showed that the proposed model is fairly accurate in predicting the device output and transfer characteristics, and can therefore, be utilized in design software involving AlGaN/GaN FinFETs.

While working on analytical models for FinFETs output characteristics, it has been realized that analytical models are quite complex in their nature and are difficult to handle from a design engineers point of view. Therefore, in the last part of the thesis, a mobility model has been developed to predict the $I-V$ characteristics of FinFETs for CAD related applications. The model integrates the device physical parameters to an $I-V$ expression, which has global validity for FinFETs made from different materials. Particle swarm optimization is used to find optimum values of model parameters, and the model is tested for devices

of varying materials and dimensions. A good agreement has been demonstrated between the modeled and experimental data.

7.1 Future Works

FinFET is a relatively new device and there are numerous avenues, which are still to be investigated for the device's better understanding and use; some of which are presented below:

1. To further improve the short channel effects by optimizing the device physical dimensions, i.e. fin height, fin thickness and gate length of the device.
2. To evaluate the maximum frequency of operation as a function of fin geometry.
3. To assess the degradation of the device target performance due to increased density of devices per unit area for VLSI technology.
4. To assess AC degradation of the device performance due to proximity effect in VLSI circuitries.
5. To develop a comprehensive tool to extract accurate device equivalent circuit parameters by using electrical response.
6. To assess intrinsic parameters of the device using DC characteristics.
7. To develop a temperature dependent FinFET DC/AC model.
8. To investigate performance of modulation doped FinFETs as a function of sheet charge density.
9. To investigate preference parameters of depletion and enhancement mode FinFETs for Hi-tech applications.

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